MYC-YZ70XX PinMapTable

版本：V1.0　20170707

Function	SoC Pin Name	Bank	Ball	Net Name	SideA	SideC	Net Name	Ball	Bank	SoC Pin Name	Function
Power-supply pins for Bank 34(HR Bank) / Input				VDDIO_34 PL	A1	C1	GND				
BANK 34 Select IO	IO_L10P_T1_34	Bank 34	V15	IO_B34_LP10	A2	C2	RGMII0_TRP0				Ethernet Data 0 Positive
BANK 34 Select IO	IO_L10N_T1_34	Bank 34	W15	IO_B34_LN10	A3	C3	RGMII0_TRN0				Ethernet Data 0 Negative
BANK 35 Select IO	IO_L23P_T3_35	Bank 35	M14	IO_B35_LP23	A4	C4	GND				
BANK 35 Select IO	IO_L23N_T3_35	Bank 35	M15	IO_B35_LN23	A5	C5	RGMII0_TRP1				Ethernet Data 1 Positive
				GND	A6	C6	RGMII0_TRN1				Ethernet Data 1 Negative
BANK 34 Select IO	IO_L6P_T0_34	Bank 34	P14	IO_B34_LP6	A7	C7	GND				
BANK 34 Select IO	IO_L6N_T0_VREF_34	Bank 34	R14	IO_B34_LN6	A8	C8	RGMII0_TRP2				Ethernet Data 2 Positive
BANK 34 Select IO	IO_L5P_T0_34	Bank 34	T14	IO_B34_LP5	A9	C9	RGMII0_TRN2				Ethernet Data 2 Negative
BANK 34 Select IO	IO_L5N_T0_34	Bank 34	T15	IO_B34_LN5	A10	C10	GND				
				GND	A11	C11	RGMII0_TRP3				Ethernet Data 3 Positive
BANK 34 Select IO	IO_L11P_T1_SRCC_34	Bank 34	U14	IO_B34_LP11	A12	C12	RGMII0_TRN3				Ethernet Data 3 Negative
BANK 34 Select IO	IO_L11N_T1_SRCC_34	Bank 34	U15	IO_B34_LN11	A13	C13	GND				
BANK 34 Select IO	IO_L9P_T1_DQS_34	Bank 34	T16	IO_B34_LP9	A14	C14	RGMII0_LED_LINK				Ethernet Link LED / Output / 1.8V IO Standard.
BANK 34 Select IO	IO_L9N_T1_DQS_34	Bank 34	U17	IO_B34_LN9	A15	C15	RGMII0_LED_ACT				Ethernet Status LED / Output / 1.8V IO Standard.
				GND	A16	C16	MDIO_CK	C10	Bank 501	PS_MIO52_501	Ethernet PHY Management data clock output / 1.8V IO Standard
BANK 34 Select IO	IO_L12P_T3_DQS_34	Bank 34	V17	IO_B34_LP21	A17	C17	MDIO_DATA	C11	Bank 501	PS_MIO53_501	Ethernet PHY Management data input/output / 1.8V IO Standard
BANK 34 Select IO	IO_L12N_T3_DQS_34	Bank 34	V18	IO_B34_LN21	A18	C18	FPGA_CONFIG_DONE	B11	Bank 0	DONE_0	Active High, DONE indicates successful completion of configuration. / Output / 3.3V IO Standard
BANK 34 Select IO	IO_L19P_T3_34	Bank 34	R16	IO_B34_LP19	A19	C19	BOOT_JP1				Boot Mode setting / See Note1
BANK 34 Select IO	IO_L19N_T3_VREF_34	Bank 34	R17	IO_B34_LN19	A20	C20	BOOT_JP2				Boot Mode setting / See Note1
				GND	A21	C21	VCCIO_500_PS				Power-supply for Peripherals of Bank 500(3.3V) / Output
Output signal used to feed watchdog				WDT_FEED_OUT	A22	C22	VCCBATT				Decryptor key memory backup supply / Input / If not used, should be tied to GND or 1.8V.
Tie this signal to WDT FEED OUT to enable watchdog; leave open to disable watchdog.				WDT_FEED_IN	A23	C23	PS_MIO39(USB1HS_D7)	C18	Bank 501	PS_MIO39_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L18P_T2_34	Bank 34	V16	IO_B34_LP18	A24	C24	PS_MIO31(USB1HS_NXT)	E16	Bank 501	PS_MIO31_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L18N_T2_34	Bank 34	W16	IO_B34_LN18	A25	C25	PS_MIO28(USB1HS_D4)	C16	Bank 501	PS_MIO28_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
				GND	A26	C26	PS_MIO30(USB1HS_STP)	C15	Bank 501	PS_MIO30_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L16P_T2_34	Bank 34	V20	IO_B34_LP16	A27	C27	PS_MIO32(USB1HS_D0)	A14	Bank 501	PS_MIO32_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L16N_T2_34	Bank 34	W20	IO_B34_LN16	A28	C28	PS_MIO33(USB1HS_D1)	D15	Bank 501	PS_MIO33_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L15P_T2_DQS_34	Bank 34	T20	IO_B34_LP15	A29	C29	PS_MIO29(USB1HS_DIR)	C13	Bank 501	PS_MIO29_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L15N_T2_DQS_34	Bank 34	U20	IO_B34_LN15	A30	C30	PS_MIO34(USB1HS_D2)	A12	Bank 501	PS_MIO34_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
				GND	A31	C31	PS_MIO38(USB1HS_D6)	E13	Bank 501	PS_MIO38_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L7P_T1_34	Bank 34	Y16	IO_B34_LP7	A32	C32	PS_MIO36(USB1HS_CLK)	A11	Bank 501	PS_MIO36_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L7N_T1_34	Bank 34	Y17	IO_B34_LN7	A33	C33	GND				
BANK 34 Select IO	IO_L17P_T2_34	Bank 34	Y18	IO_B34_LP17	A34	C34	PS_MIO35(USB1HS_D3)	F12	Bank 501	PS_MIO35_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
BANK 34 Select IO	IO_L17N_T2_34	Bank 34	Y19	IO_B34_LN17	A35	C35	PS_MIO37(USB1HS_D5)	A10	Bank 501	PS_MIO37_501	Bank 501 MIO / USB1 Controller Signal by default / 1.8V IO Standard
				GND	A36	C36	SDIO0_CMD	C17	Bank 501	PS_MIO41_501	SDIO Command / 1.8V IO Standard
BANK 34 Select IO	IO_L24P_T3_34	Bank 34	P15	IO_B34_LP24	A37	C37	SDIO0_CD	D16	Bank 501	PS_MIO46_501	SDIO Card Detection / 1.8V IO Standard
BANK 34 Select IO	IO_L24N_T3_34	Bank 34	P16	IO_B34_LN24	A38	C38	SDIO0_D4	B15	Bank 501	PS_MIO45_501	SDIO Data 4 / 1.8V IO Standard
BANK 34 Select IO	IO_L22P_T3_34	Bank 34	W18	IO_B34_LP22	A39	C39	SDIO0_CLK	D14	Bank 501	PS_MIO40_501	SDIO Clock / 1.8V IO Standard
BANK 34 Select IO	IO_L22N_T3_34	Bank 34	W19	IO_B34_LN22	A40	E40	GND				
				GND	A41	C41	SDIO0_D3	F13	Bank 501	PS_MIO44_501	SDIO Data 3 / 1.8V IO Standard
BANK 34 Select IO	IO_L12P_T1_MRCC_34	Bank 34	U18	IO_B34_LP12	A42	C42	SDIO0_D1	E12	Bank 501	PS_MIO42_501	SDIO Data 1 / 1.8V IO Standard
BANK 34 Select IO	IO_L12N_T1_MRCC_34	Bank 34	U19	IO_B34_LN12	A43	C43	SDIO0_D2	A9	Bank 501	PS_MIO43_501	SDIO Data 2 / 1.8V IO Standard
BANK 34 Select IO	IO_L20P_T3_34	Bank 34	T17	IO_B34_LP20	A44	C44	UART1_TX	B12	Bank 501	PS_MIO48_501	Debug UART TX / 1.8V IO Standard
BANK 34 Select IO	IO_L20N_T3_34	Bank 34	R18	IO_B34_LN20	A45	C45	UART1_RX	C12	Bank 501	PS_MIO49_501	Debug UART RX / 1.8V IO Standard
				GND	A46	C46	EXT_RST_IN				Active-low signal Used for system reset / Input / 3.3V IO Standard
BANK 34 Select IO	IO_L23P_T3_34	Bank 34	N17	IO_B34_LP23	A47	C47	PS_500_RESET_OUTn	D8	Bank 500	PS_MIO7_500	Set low to reset peripherals / Output / 3.3V IO Standard
BANK 34 Select IO	IO_L23N_T3_34	Bank 34	P18	IO_B34_LN23	A48	C48	FPGA_CONFIG_RESET	L6	Bank 0	PROGRAM_B_0	Active Low, asynchronous reset to configuration logic. / Input / 3.3V IO Standard
BANK 34 Select IO	IO_L14P_T2_SRCC_34	Bank 34	N20	IO_B34_LP14	A49	E49	XADC_VCC				XADC analog supply voltage(1.8V). / Output for Peripherals.
BANK 34 Select IO	IO_L14N_T2_SRCC_34	Bank 34	P20	IO_B34_LN14	A50	C50	XADC_GND				XADC analog ground
				GND	A51	C51	Sys_PG				Open-Drain output signal, high voltage indicates SOM Power Good.
BANK 35 Select IO	IO_L8P_T1_AD10P_35	Bank 35	M17	IO_B35_LP8	A52	E52	VCCIO_501_PS				Power-supply for Peripherals of Bank 501(1.8V) / Output
BANK 35 Select IO	IO_L8N_T1_AD10N_35	Bank 35	M18	IO_B35_LN8	A53	C53	GND				
BANK 34 Select IO	IO_L13P_T2_MRCC_34	Bank 34	N18	IO_B34_LP13	A54	C54	VDD_5V				DC5V　PowerSupply / Input
BANK 34 Select IO	IO_L13N_T2_MRCC_34	Bank 34	P19	IO_B34_LN13	A55	C55	VDD_5V				DC5V　PowerSupply / Input

Function	SoC Pin Name	Bank	Ball	Net Name	SideB	SideD	Net Name	Ball	Bank	SoC Pin Name	Function
Power-supply pins for Bank 35(HR Bank) / Input				VDDIO_35_PL	B1	D1	GND				
BANK 35 Select IO	IO_L7P_T1_AD2P_35	Bank 35	M19	IO_B35_LP7	B2	D2	JTAG_TCK	F9	Bank 0	TCK_0	JTAG Test Clock / 3.3V IO Standard
BANK 35 Select IO	IO_L7N_T1_AD2N_35	Bank 35	M20	IO_B35_LN7	B3	D3	JTAG_TDI	G6	Bank 0	TDI_0	JTAG Test Data Input / 3.3V IO Standard
BANK 35 Select IO	IO_L21P_T3_DQS_AD14P_35	Bank 35	N15	IO_B35_LP21	B4	D4	JTAG_TDO	F6	Bank 0	TDO_0	JTAG Test Data Output / 3.3V IO Standard
BANK 35 Select IO	IO_L21N_T3_DQS_AD14N_35	Bank 35	N16	IO_B35_LN21	B5	D5	JTAG_TMS	J6	Bank 0	TMS_0	JTAG Test Mode Select / 3.3V IO Standard
				GND	B6	D6	GND				
BANK 35 Select IO	IO_L12P_T1_MRCC_35	Bank 35	K17	IO_B35_LP12	B7	D7	IO_B35_LP6	F16	Bank 35	IO_L6P_T0_35	BANK 35 Select IO
BANK 35 Select IO	IO_L12N_T1_MRCC_35	Bank 35	K18	IO_B35_LN12	B8	D8	IO_B35_LN6	F17	Bank 35	IO_L6N_T0_VREF_35	BANK 35 Select IO
BANK 35 Select IO	IO_L9P_T1_DQS_AD3P_35	Bank 35	L19	IO_B35_LP9	B9	D9	IO_B35_LP5	E18	Bank 35	IO_L5P_T0_AD9P_35	BANK 35 Select IO
BANK 35 Select IO	IO_L9N_T1_DQS_AD3N_35	Bank 35	L20	IO_B35_LN9	B10	D10	IO_B35_LN5	E19	Bank 35	IO_L5N_T0_AD9N_3	BANK 35 Select IO
				GND	B11	D11	GND				
BANK 35 Select IO	IO_L17P_T2_AD5P_35	Bank 35	J20	IO_B35_LP17	B12	D12	IO_B35_LP4	D19	Bank 35	IO_L4P_T0_35	BANK 35 Select IO
BANK 35 Select IO	IO_L17N_T2_AD5N_35	Bank 35	H20	IO_B35_LN17	B13	D13	IO_B35_LN4	D20	Bank 35	IO_L4N_T0_35	BANK 35 Select IO
BANK 35 Select IO	IO_L14P_T2_AD4P_SRCC_35	Bank 35	J18	IO_B35_LP14	B14	D14	IO_B35_LP1	C20	Bank 35	IO_L1P_T0_AD0P_35	BANK 35 Select IO
BANK 35 Select IO	IO_L14N_T2_AD4N_SRCC_35	Bank 35	H18	IO_B35_LN14	B15	D15	IO_B35_LN1	B20	Bank 35	IO_L1N_T0_AD0N_35	BANK 35 Select IO
				GND	B16	D16	GND				
BANK 35 Select IO	IO_L22P_T3_AD7P_35	Bank 35	L14	IO_B35_LP22	B17	D17	IO_B35_LP3	E17	Bank 35	IO_L3P_T0_DQS_AD1P_35	BANK 35 Select IO
BANK 35 Select IO	IO_L22N_T3_AD7N_35	Bank 35	L15	IO_B35_LN22	B18	D18	IO_B35_LN3	D18	Bank 35	IO_L3N_T0_DQS_AD1N_35	BANK 35 Select IO
BANK 35 Select IO	IO_L24P_T3_AD15P_35	Bank 35	K16	IO_B35_LP24	B19	D19	IO_B35_LP2	B19	Bank 35	IO_L2P_T0_AD8P_35	BANK 35 Select IO
BANK 35 Select IO	IO_L24N_T3_AD15N_35	Bank 35	J16	IO_B35_LN24	B20	D20	IO_B35_LN2	A20	Bank 35	IO_L2N_T0_AD8N_35	BANK 35 Select IO
				GND	B21	D21	GND				
BANK 35 Select IO	IO_L10P_T1_AD11P_35	Bank 35	K19	IO_B35_LP10	B22	D22	IO_B35_LP20	K14	Bank 35	IO_L20P_T3_AD6P_35	BANK 35 Select IO
BANK 35 Select IO	IO_L10N_T1_AD11N_35	Bank 35	J19	IO_B35_LN10	B23	D23	IO_B35_LN20	J14	Bank 35	IO_L20N_T3_AD6N_35	BANK 35 Select IO
BANK 35 Select IO	IO_L18P_T2_AD13P_35	Bank 35	G19	IO_B35_LP18	B24	D24	IO_B35_LP11	L16	Bank 35	IO_L11P_T1_SRCC_35	BANK 35 Select IO
BANK 35 Select IO	IO_L18N_T2_AD13N_35	Bank 35	G20	IO_B35_LN18	B25	D25	IO_B35_LN11	L17	Bank 35	IO_L11N_T1_SRCC_35	BANK 35 Select IO
				GND	B26	D26	GND				
BANK 35 Select IO	IO_L15P_T2_DQS_AD12P_35	Bank 35	F19	IO_B35_LP15	B27	D27	IO_B34_LP1	T11	Bank 34	IO_L1P_T0_34	BANK 34 Select IO
BANK 35 Select IO	IO_L15N_T2_DQS_AD12N_35	Bank 35	F20	IO_B35_LN15	B28	D28	IO_B34_LN1	T10	Bank 34	IO_L1N_T0_34	BANK 34 Select IO
BANK 35 Select IO	IO_L13P_T2_MRCC_35	Bank 35	H16	IO_B35_LP13	B29	D29	IO_B34_LP2	T12	Bank 34	IO_L2P_T0_34	BANK 34 Select IO
BANK 35 Select IO	IO_L13N_T2_MRCC_35	Bank 35	H17	IO_B35_LN13	B30	D30	IO_B34_LN2	U12	Bank 34	IO_L2N_T0_34	BANK 34 Select IO
				GND	B31	D31	GND				
BANK 35 Select IO	IO_L16P_T2_35	Bank 35	G17	IO_B35_LP16	B32	D32	IO_B34_LP4	V12	Bank 34	IO_L4P_T0_34	BANK 34 Select IO
BANK 35 Select IO	IO_L16N_T2_35	Bank 35	G18	IO_B35_LN16	B33	D33	IO_B34_LN4	W13	Bank 34	IO_L4N_T0_34	BANK 34 Select IO
BANK 35 Select IO	IO_L19P_T3_35	Bank 35	H15	IO_B35_LP19	B34	D34	IO_B34_LP3	U13	Bank 34	IO_L3P_T0_DQS_PUDC_B_34	BANK 34 Select IO
BANK 35 Select IO	IO_L19N_T3_VREF_35	Bank 35	G15	IO_B35_LN19	B35	D35	IO_B34_LN3	V13	Bank 34	IO_L3N_T0_DQS_34	BANK 34 Select IO

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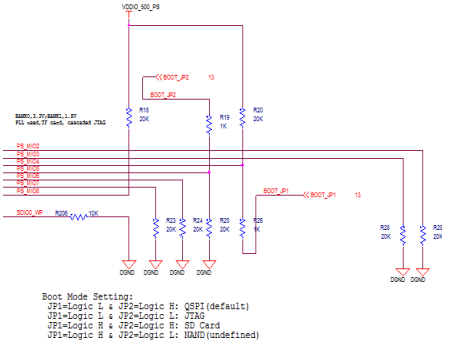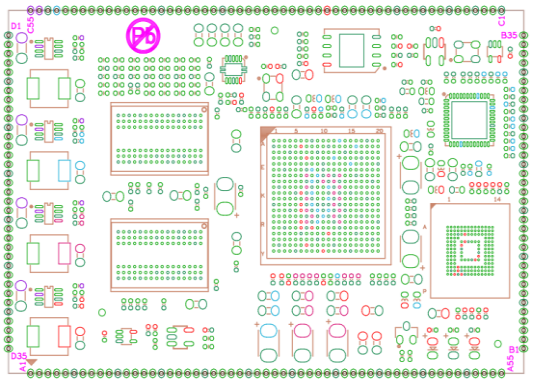
Note 1:Boot mode setting