FZ3 Deep Learning Accelerator Card Hardware Manual

Version V1.0

Revision History

Version	Description	Date
V1.0	Initial Version	2020/06/23

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Chapter 1 Overview

1.1 Product Description

The FZ3 Deep learning computing card is an embedded intelligent AI development platform with Xilinx XCZU3EG as the core launched by Shenzhen Myir Technology Co., Ltd. Using Xilinx's latest 16nm process-based Xilinx Zynq UltraScale + MPSoC platform, integrated quad-core Cortex ™ -A53 processor, dual-core Cortex ™ -R5 real-time processing unit and Mali-400 MP2 graphics processing unit and 16nm FinFET + programmable logic The heterogeneous processing system has high performance, low power consumption, high expansion and other characteristics, and can meet various needs in industrial design.

At the same time, Shenzhen Myir Technology Co., Ltd. provides a variety of mature hardware solutions, provides a wealth of embedded operating system software resources, through supporting design tools to help embedded developers give full play to the synergy of hardware and software to achieve innovation beyond traditional architecture design.

1.2 Picture

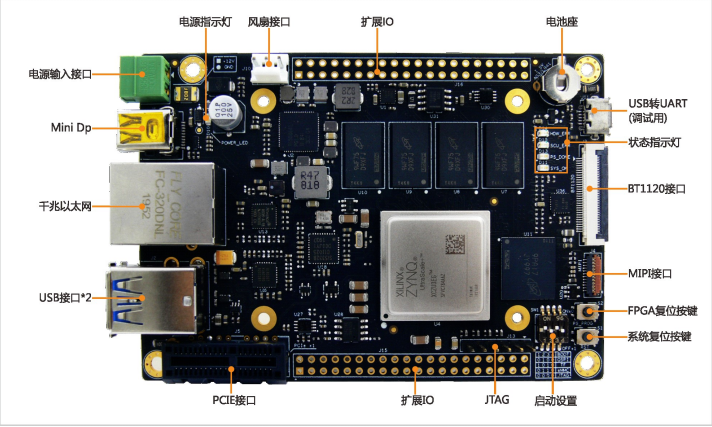


Figure 1-2

Product difference	
FZ3A	2GB DDR4 64bit 2400Mbps
FZ3B	4GB DDR4 64bit 2400Mbps

Chapter 2 SOC introduction

2.1 SoC features

The XCZU3EG used in this development platform belongs to the Zynq UltraScale + MPSoC series SoC, integrating ARM quad-core Cortex-A53 (PS), dual-core Cortex-R5 (PS), Mali-400 MP2 graphics processing unit and Kintex Ultrascale + FPGA (PL). The quad-core Cortex-A53 has powerful computing capabilities, the dual-core Cortex-R5 can be used for real-time processing applications, the Mali-400 MP2 can be used to accelerate graphics processing, and the FPGA is fully programmable. With the expandable I / O ports, it can adapt to a variety of application AI development scenarios. The main chip of the AI development platform uses Xilinx XCZU3EG-SFVC784 devices with a speed grade of -1 (MYC-CZU3EG SOM is designed to support all speed grades of XCZU3EG-SFVC784 devices). XCZU3EG-SFVC784 supports 1.5GHz (max -1) APU speed, 600MHz (max -1) RPU speed, 667MHz (max -1) GPU speed, and DDR4 speed up to 2400Mbps. The XCZU3EG-SFVC784 device has the following resources:

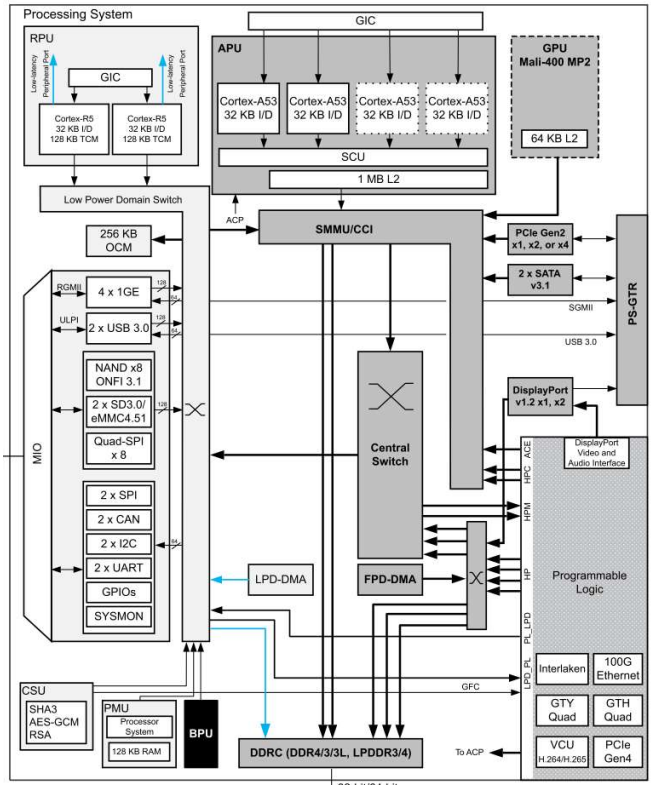


Figure 2-1

- **Processing System (PS)**
  - **Processor Core:** Quad-core ARM Cortex-A53 MPCore up to 1.5GHz
  - **Maximum Frequency:** 1.5Ghz
  - **APU:** L1 Cache 32KB I / D per core, L2 Cache 1MB.
  - **RPU：** L1 Cache 32KB I / D per core.
  - **On-Chip Memory:** 256 KB
  - **External Memory:** LPDDR4， DDR4， DDR3, DDR3L LPDDR3 with ECC
  - **External Static Memory:** 2x Quad-SPI, NAND, NOR
  - **DMA Channels:** 8 Programmable Logic（4 for PL）
  - **Peripherals:**
    - High speed: PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet.
    - Regular speed: 2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
- **Programmable Logic (PL)**

	MYC-XCZU3EG
Logic Equivalent	Xilinx Kintex Ultrascale+®FPGA
Programmable Logic Cells	154K
Look-Up Tables	71K
Flip-Flops	141K
Block RAM	Distributed RAM 1.8Mb / Block RAM 7.6Mb
DSP slice	360
AMS-System Monitor	1

Table 2-1

2.2 SoC BANK

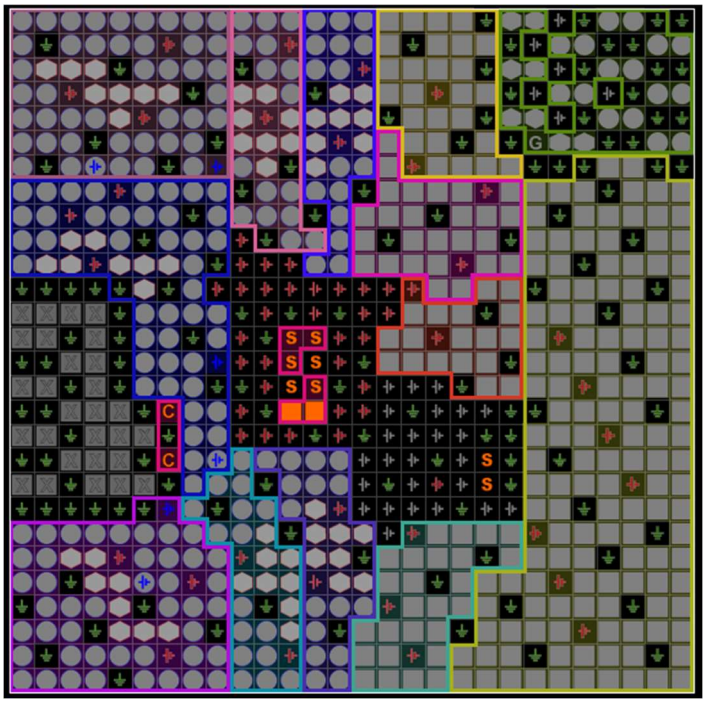


Figure 2-2 XCZU3EG SFVC784 Banks

- **BANK 0 :** humidity Sensor, XADC , Other configuration signals
- **BANK 24： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 25： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 26： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 44： PL** HD BANK, 24Pin(12 pairs of differential signal)
- **BANK 64： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 65： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 66： PL** HP BANK, 52Pin(26 pairs of differential signal)
- **BANK 500:** PS side, MIO[00:25] 26pin， multiplex pin
- **BANK 501:** PS side, MIO[26:51] 26pin， multiplex pin
- **BANK 502:** PS side, MIO[52:77] 26pin， multiplex pin
- **BANK 503:** PS side, PS configuration pin, includeJTAG boot configuration reset, etc.
- **BANK 504:** PS side, DDR BANK
- **BANK 505:** PS side, MGTR BANK

Chapter 3 Onboard Resources

3.1 Hardware resources

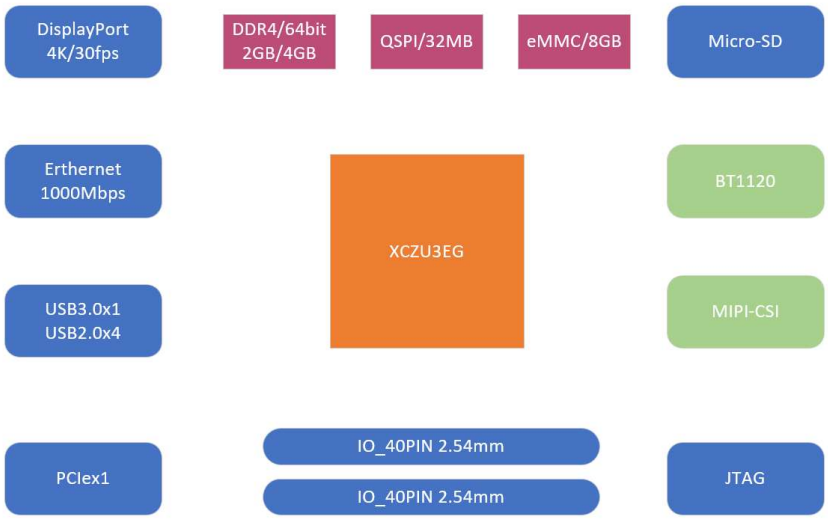


Figure 3-1

➢ Hardware resources

- 2GB/4GB DDR4 SDRAM（64bit 2400Mbps）
- 8GB eMMC
- 32MB QSPI
- Gigabit Ethernet
- RS485*1，CAN*1

➢ Peripheral interface and resources

- 1 Channel SD/MMC interface
- 1 Channel USB2.0 tyepA，1 Channel USB3.0 typeA
- 1 Channel RJ45 Ethernet interface
- 1 Channel Mini Displayport interface
- 1 Channel PCIe x1 interface
- 1 system reset key，1 FPGA reset key

- 1 Channel MIPI-CSI interface，1 Channel BT1120 interface
- 1 Channel JTAG interface，1 Channel USB to UART debug interface
- 2 Channel 40PIN 2.54mm spacing IO expander
- 4 onboard LED status indicators

3.2 Boot Mode & JTAG Mode

The development board provides two boot modes by default. Users can select to boot the system from the TF CARD or the QSPI flash. For detailed information, refer to the table below.

Name	PS_MODE0	PS_MODE1	PS_MODE2	PSMODE3
SW1	M0	M1	M2	/
JTAG	ON	ON	ON	/
QSPI32	ON	OFF	ON	/
SD1	OFF	ON	OFF	/
eMMC	ON	OFF	OFF	/

Table 3-2

PS: OFF=1.ON=0

3.3 DDR4

The development Board incorporates four Micron DDR4 memory chips (MT40A256M16LY-062E IT:F) forming a 256M x 64-bit interface with a total of 2GB RAM(optional 4GB). The DDR4 memorys are connected to the memory controller in the PS of the Zynq® UltraScale+™ MPSoC, which supports access speed up to 2400 MT/s。

3.4 Storage

3.4.1 SPI Flash

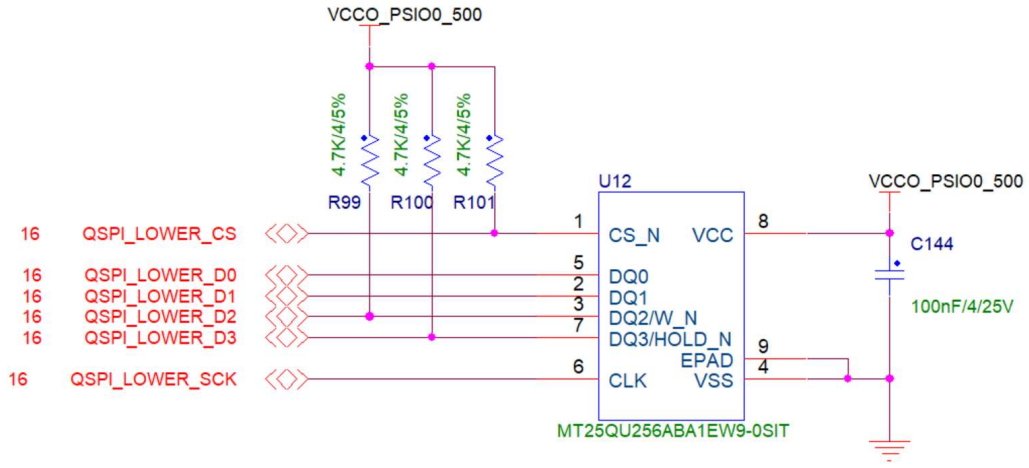


Figure 3-4-1

The development Board incorporates 1 Quad-SPI Flash(MT25QU256ABA1EW9-0SIT)，Connect to the QSPI0 interface of the CPU—PS_MIO0 ~ PSMIO5 pins of BANK500:

U12	
PS_MIO0	QSPI_LOWER_SCK
PS_MIO1	QSPI_LOWER_D1
PS_MIO2	QSPI_LOWER_D2
PS_MIO3	QSPI_LOWER_D3
PS_MIO4	QSPI_LOWER_D0
PS_MIO5	QSPI_LOWER_CS

Table 3-4-1

It can be used to initialize the PS subsystem and configure the PL subsystem (bitstream).

3.4.2 eMMC

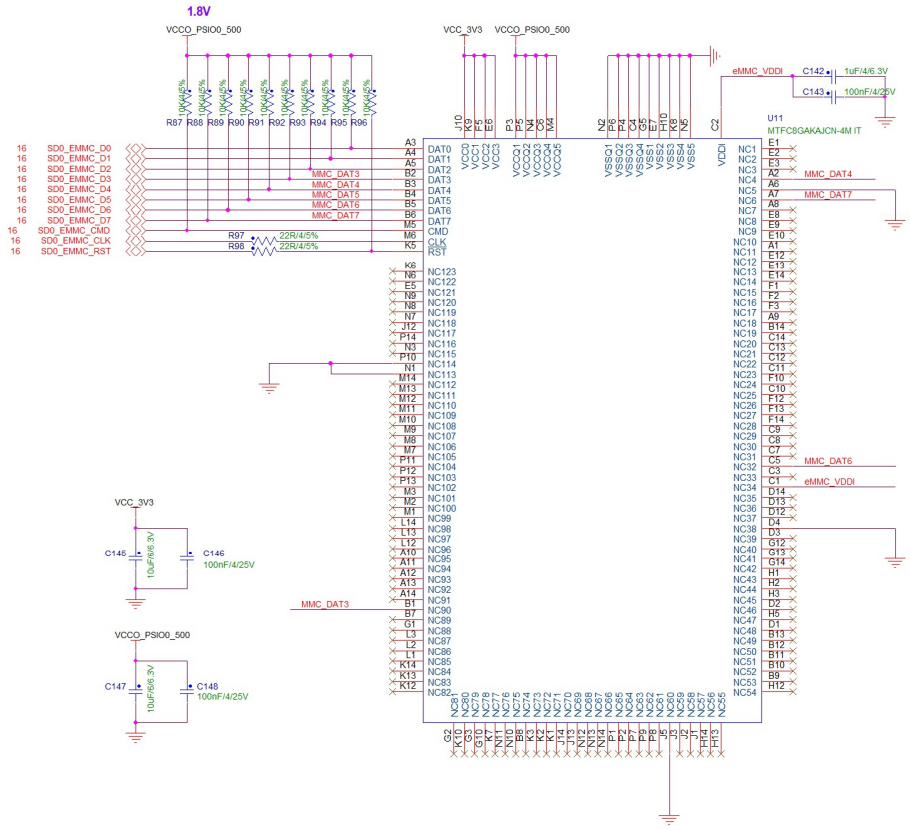


Figure 3-4-2

Onboard Micron 8GB eMMC -- MTFC8GAKAJCN-4M IT，8 bit interface，Connectted to CPU SDIO1-- PS_MIO13 ~ PS_MIO23 pins of BANK500:

U31	
PS_MIO13	SD0_EMMC_D0
PS_MIO14	SD0_EMMC_D1
PS_MIO15	SD0_EMMC_D2
PS_MIO16	SD0_EMMC_D3
PS_MIO17	SD0_EMMC_D4
PS_MIO18	SD0_EMMC_D5
PS_MIO19	SD0_EMMC_D6
PS_MIO20	SD0_EMMC_D7
PS_MIO21	SD0_EMMC_CMD
PS_MIO22	SD0_EMMC_CLK
PS_MIO23	SD0_EMMC_RST

Table 3-4-2

3.5 Erthernet

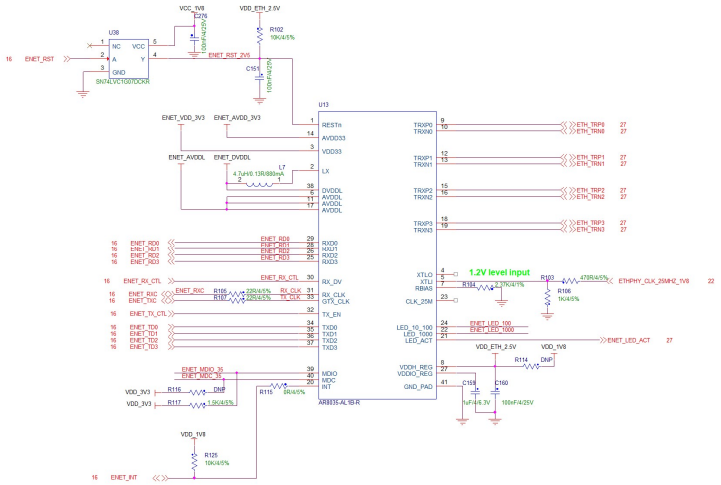


Figure 3-5

The PS unit of Zynq UltraScale + contains a Gigabit Ethernet MAC hardware controller, and an Ethernet physical layer transmission chip needs to be connected to the outside. The development board uses AR8035-AL1B-R as the PHY, and uses the PS RGMII interface to connect a Gigabit Ethernet mouth. The IIC address of PHY is 0x4.

AR8035-AL1B-R is connected to the PS_MIO64 ~ PS_MIO77 pins of the CPU's ETH0-BANK501:

U34	
PS_MIO64	ENET_TXC
PS_MIO65	ENET_TD0
PS_MIO66	ENET_TD1
PS_MIO67	ENET_TD2
PS_MIO68	ENET_TD3
PS_MIO69	ENET_TX_CTL
PS_MIO70	ENET_RXC
PS_MIO71	ENET_RD0
PS_MIO72	ENET_RD1
PS_MIO73	ENET_RD2
PS_MIO74	ENET_RD3
PS_MIO75	ENET_RX_CTL
PS_MIO76	ENET_MDC_35
PS_MIO77	ENET_MDIO_35
PS_MIO39	ENET_INT
PS_MIO40	GEM3_RESET_N

Table 3-5

3.6 USB

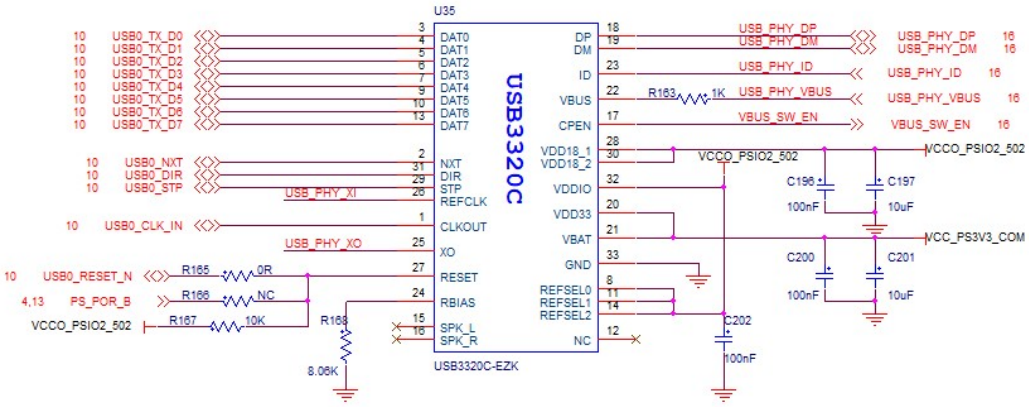


Figure 3-6

Zynq ’s PS-side USB controller is connected to a SMSC company ’s USB PHY chip USB3320C to form a USB 2.0 port as a USB Host, and then expands four USB2.0 ports through GL852G. One of the port signals is combined with the PS 3.0 USB port Together form a USB3.0 port, and several other ports are led out as separate USB2.0 ports.

USB3320C is connected to the PS_MIO52 ~ PS_MIO63 pins of the USB0-BANK501 of the CPU.

U35	
PS_MIO52	USB0_CLK_IN
PS_MIO53	USB0_DIR
PS_MIO54	USB0_TX_D2
PS_MIO55	USB0_NXT
PS_MIO56	USB0_TX_D0
PS_MIO57	USB0_TX_D1
PS_MIO58	USB0_STP
PS_MIO59	USB0_TX_D3
PS_MIO60	USB0_TX_D4
PS_MIO61	USB0_TX_D5
PS_MIO62	USB0_TX_D6
PS_MIO63	USB0_TX_D7
PS_MIO38	USB0_RESET_N

Table 3-6

3.7 Multi-channel programmable clock generator

This development platform has a programmable IDT SI5332 I2C programmable clock generator. This clock IC generates the necessary clock for the entire system through external 26 MHz crystal oscillator after frequency multiplication and frequency division processing. The schematic diagram is as follows:

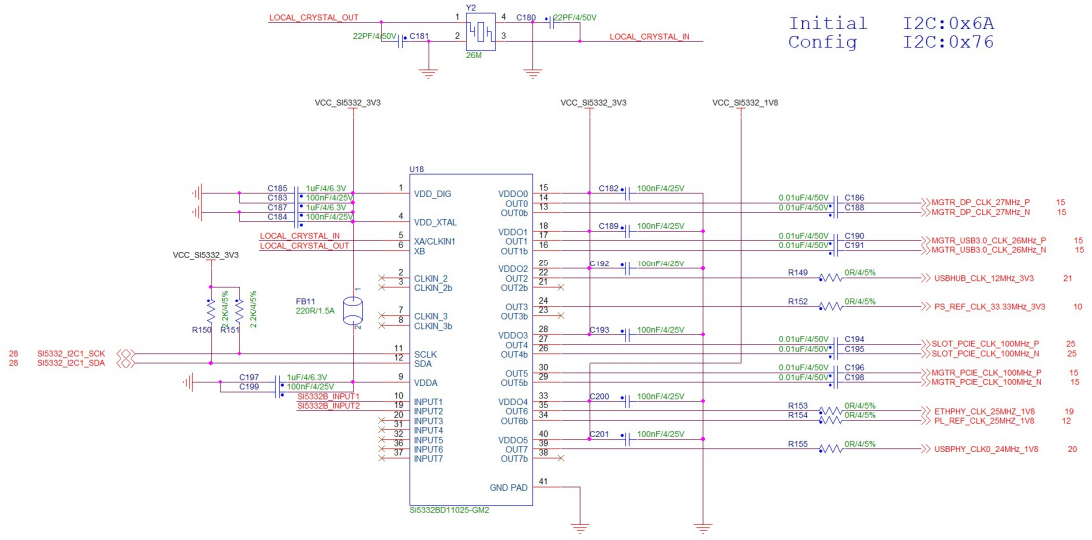


Figure 3-7-1

3.8 External watchdog and reset

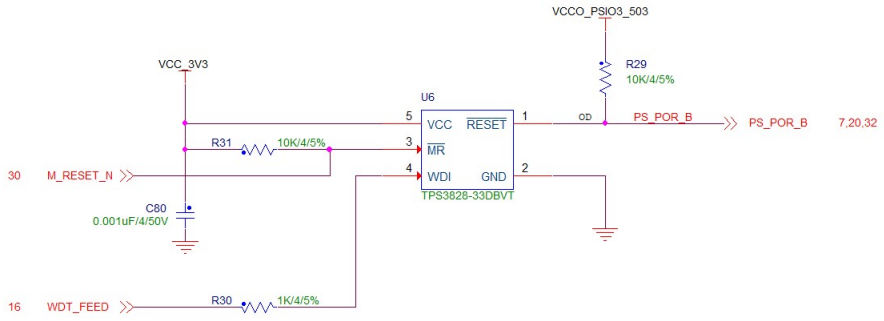


Figure 3-8-1

The development platform uses an external watchdog chip TPS3828-33DBVT. The dog feed pin of this chip is connected to the PS_MIO41 pin of the CPU. When PS_MIO41 is

set to high impedance, the watchdog does not work. You can set PS_MIO41 to high impedance during the debugging phase Watchdog work is prohibited.

The TPS3828-33DBVT also has the function of monitoring the voltage reset system. When the power supply voltage reaches the threshold voltage, the reset automatically pulls up to start the system. The reset signal is connected to ZU3EG, which can directly reset the main chip.

Chapter 4 Hardware Introduction

4.1 Interface summary

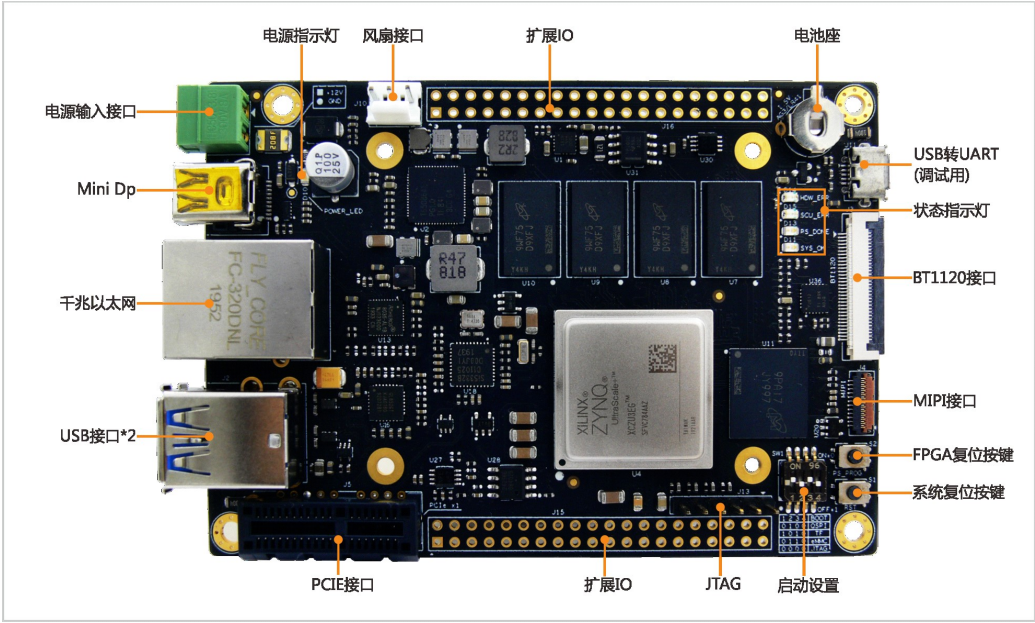


Figure 4-1

Num	Description
J1	Power input(12V/2A)
J6	DisplayPort （PS）
J8	Gigabyte Erthnet（PS）
J2	1xUSB3.0 +1xUSB2.0（PS）
J5	PCIe x1（PS）
J12	TF Card（PS）
J3	BT1120 video input（PL）
J4	MIPI-CSI image input（PL）
J13	JTAG
J11	MicroUSB to UART debug port（PS）
J9	Bat connector
J10	Fan connector
J15，J16	Expansion IO

Table 4-1

4.2 PS Unit

4.2.1 DisplayPort

One DisplayPort 1.2a interface, led from PS-side GTR, supports 4K / 30fps video output. The port is J6.

4.2.2 PCIe 1x

One PCIe 1x interface, led from PS-side GTR, supports PCIe 2.1. The port is J5.

4.2.3 Erthernet

One 10/100 / 1000Mbps Ethernet RJ45 interface, the port is J8.

4.2.4 USB3.0 HOST

One USB 2.0 interface(up), 1 USB3.0 interface (down), led out through the double-layer USB3.0 TYPE-A interface on the board, as HOST, the interface is J2.

4.2.5 TF Card

One TF card slot, used for boot or storage, the interface is J12.

4.2.6 MicroUSB to UART

One MicroUSB to UART interface for debugging, the interface is J11.

4.2.7 JTAG

One 14 Pin ARM standard JTAG, can debug PS and PL unit, you can see the signal definition on the bottom of the PCB, the port is J13.

4.3 PL Unit

4.3.1 MIPI-CSI

This development board has a MIPI-CSI interface on the PL end, and the MIPI signal directly passes through the IO on the PL end and enters the FPGA for decoding. For detailed IO details, please refer to the PINMAP. Interface bit J4.。

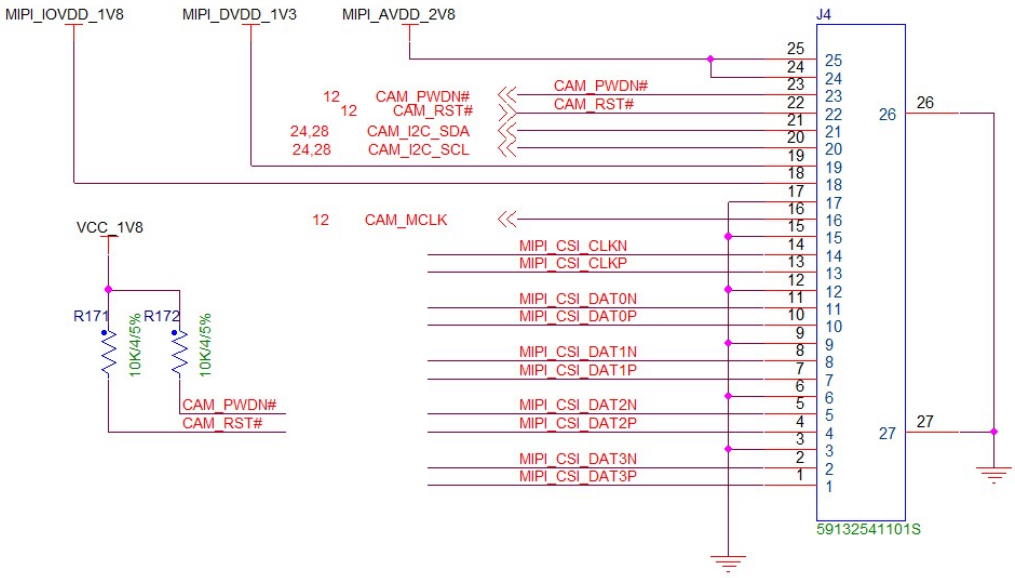


Figure 4-3-1

4.3.2 BT1120

This development board has a BT1120 video input interface on the PL end. The BT1120 video signal directly passes through the IO on the PL end and enters the FPGA to be decoded by unique logic. For detailes about the IO, please refer to the PINMAP，the interface is J3.

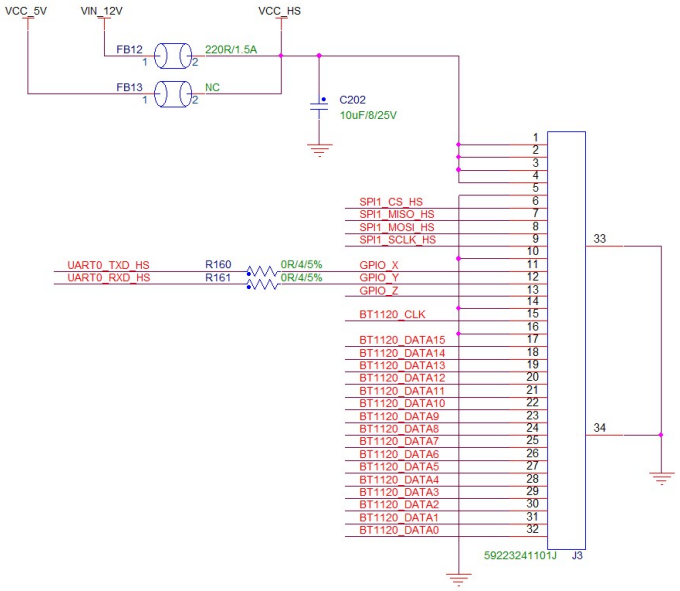


Figure 4-3-2

4.3.3 Expansion IO

This development board uses two 2x20PIN 2.54 pin headers for IO expansion, including 12V, 5V, 3.3V, 1.8V and other power output, CAN, RS485, USB2.0x2, 4xPSMIO, 40PIN PL terminal IO and other signals. The interfaces are J15 and J16. For the detailed signal definition and details, please refer to the schematic diagram and the ROUTE length form. The applicable connector specifications are in the CD-ROM.

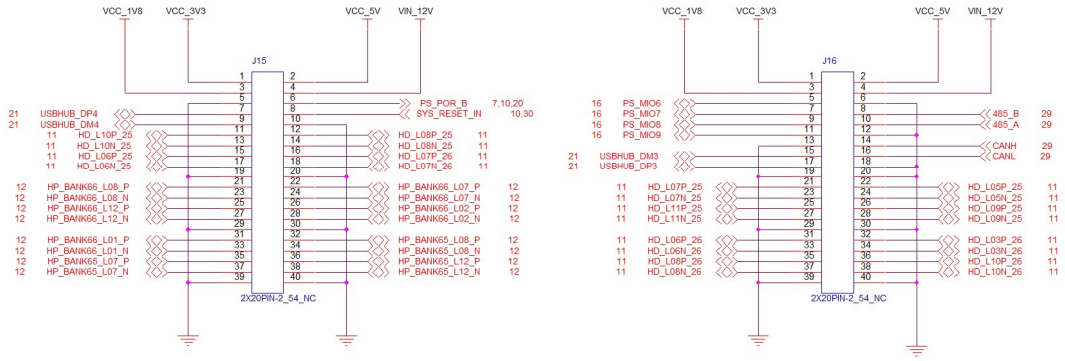


Figure 4-3-2

4.4 Other interface

4.4.1 Power input

The power input interface of this development board defaults to 12V input, and the overcurrent protection is 2A. It is recommended to use 12V / 2A power input. The interface is J1.

4.4.2 RTC bat connector

This development board has left RTC battery interface, can use 1.5V AG3 / LR41 type battery, the interface is J9.

4.4.3 Fan connector

This development board has a fan interface, which is powered by 12V by default. The fan speed can be detected through the PL terminal IO. The interface is J10.

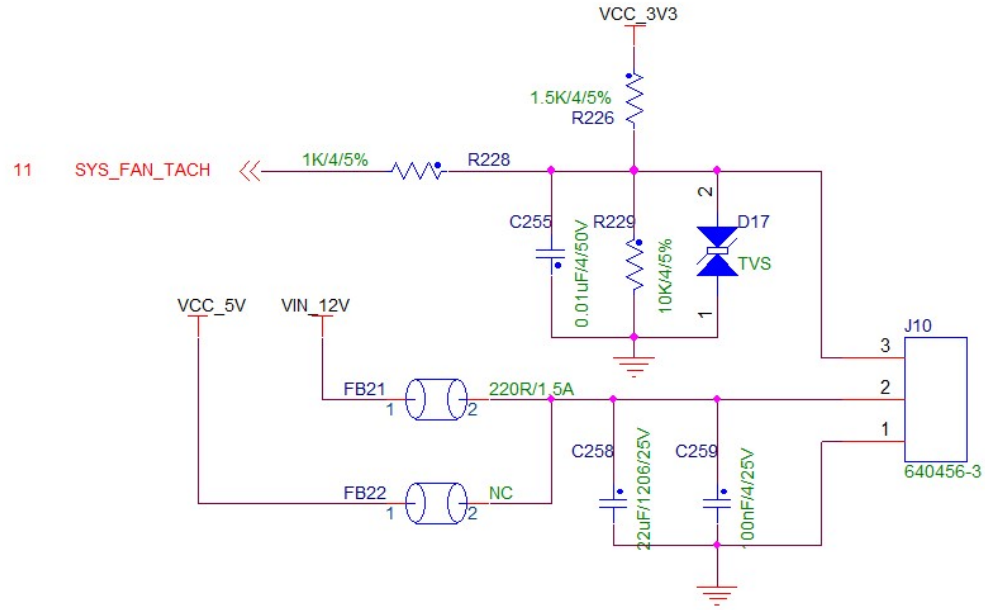


Figure 4-4-3

4.4.4 CAN

This board has an CAN interface, and signals are drawn from pins 14 and 16 of interface J16.

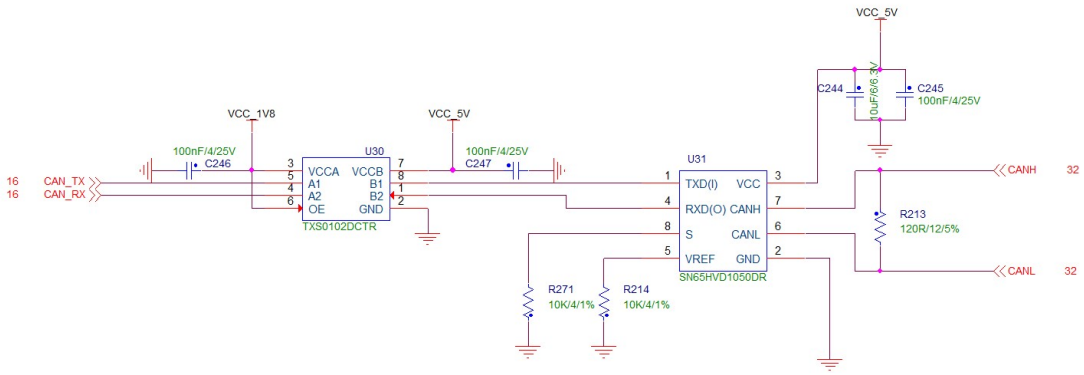


Figure 4-4-4

4.4.5 RS485

This development board has an RS485 interface, and signals are drawn from pins 8 and 10 of interface J16.

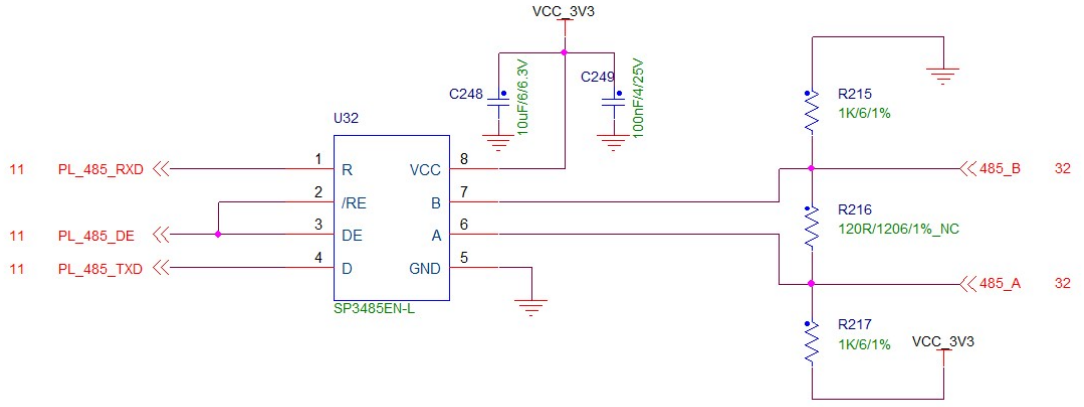
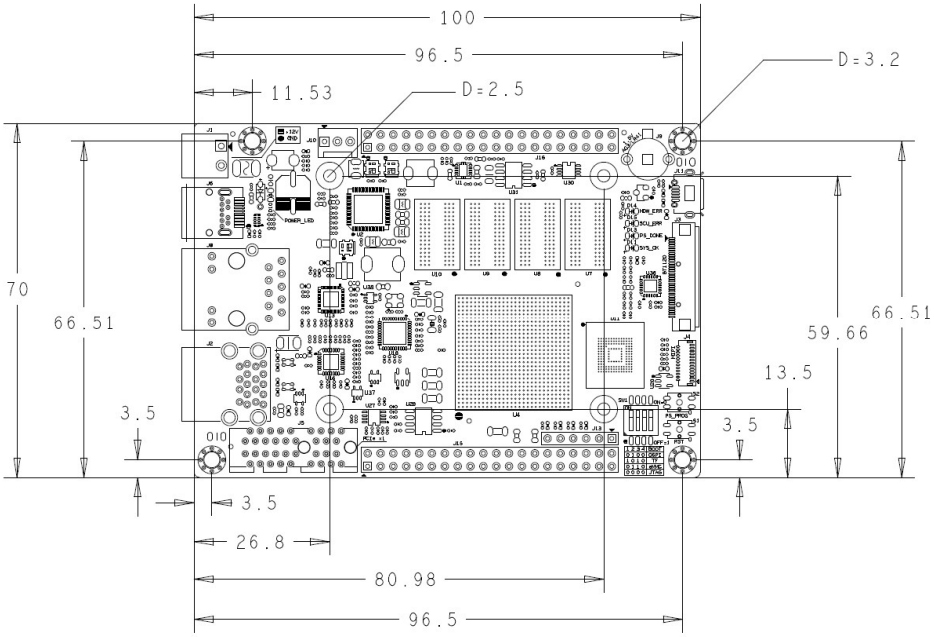


Figure 4-4-5

! CAUTION: For the specific access pins of the signal, please refer to the PINMAP table in the CD. There are detailed definitions and related trace length data.

Chapter 5 Mechanical parameters



- Operating Temperature:
  - -40~+85 ℃, Industrial grade(default)
  - 0~+ 70 ℃, Commercial grade
- Humidity: 20%~90%
- Power Supply: 12V (Limited support 6V-12.6V)
- Expansion IO: Two 40pin 2.54 spacing dip connector
- PCB: 12 Layer, Immersion Gold, Lead free
- Dimensions:
  - PCB: 100mm x 70mm
  - FAN: 60mm x 52mm

Appendix 1 Warranty & Technical Support Services

MYIR Tech Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always

four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:
1. Technical support service

a) MYIR offers technical support for the hardware and software materials which have provided to customers;
b) To help customers compile and run the source code we offer;
c) To help customers solve problems occurred during operations if users follow the user manual documents;
d) To judge whether the failure exists;
e) To provide free software upgrading service.

However, the following situations are not included in the scope of our free technical support service:

a) Hardware or software problems occurred during customers' own development;
b) Problems occurred when customers compile or run the OS which is tailored by themselves;
c) Problems occurred during customers' own applications development;
d) Problems occurred during the modification of MYIR's software source code.

2. After-sales maintenance service
The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

a) The warranty period is expired;
b) The customer cannot provide proof-of-purchase or the product has no serial number;

c) The customer has not followed the instruction of the manual which has caused the damage the product;

d) Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;

e) Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;

f) Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;

g) Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

1) MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
2) Please do not use finger nails or hard sharp object to touch the surface of the LCD.
3) MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
4) Do not clean the surface of the screen with chemicals.
5) Please read through the product user manual before you using MYIR's products.
6) For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

3. Maintenance period and charges

a) MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

b) For products within warranty period and caused by quality problem, MYIR offers free

maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

4. Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

5. Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

1. MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
2. MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
3. MYIR provides other products supporting services like power adapter, LCD panel, etc.
4. ODM/OEM services.

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