Schematic: MYB-C437X-PRU

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Title: MYB-C437X_PRU

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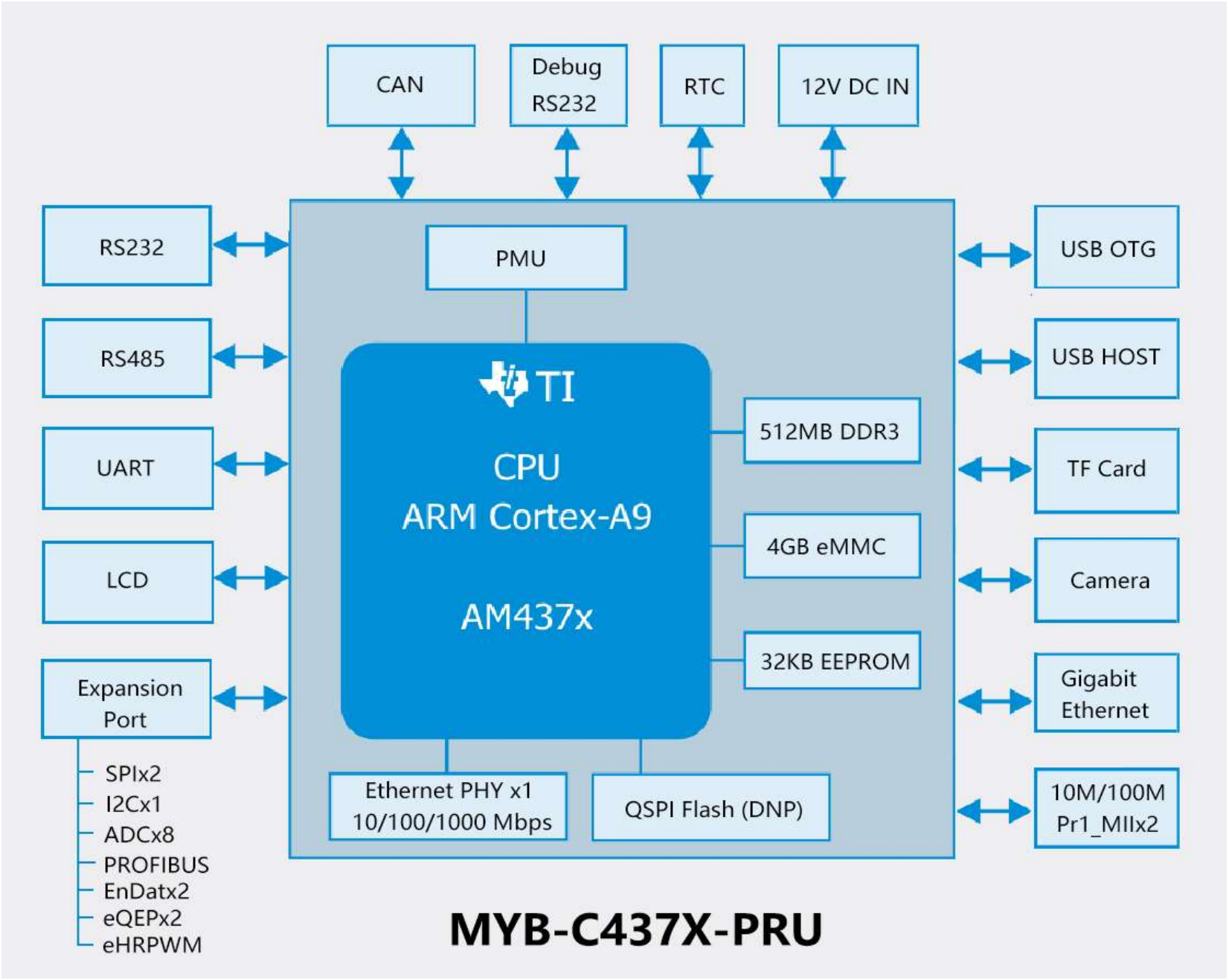

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Size: A3	Document Number: BLock Diagram	Rev: V1.1
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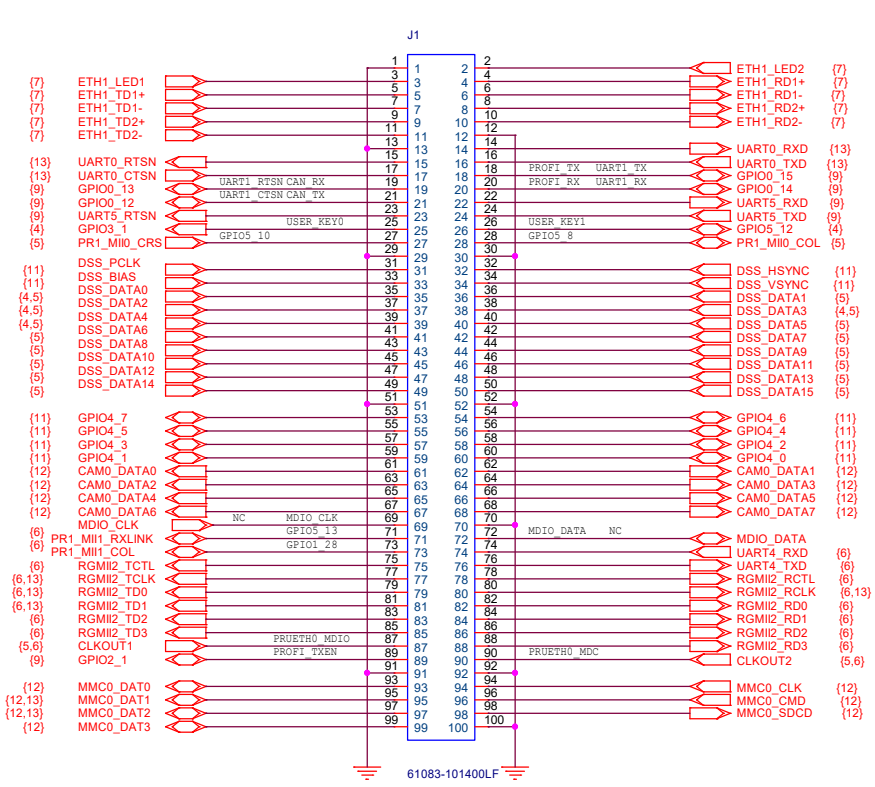

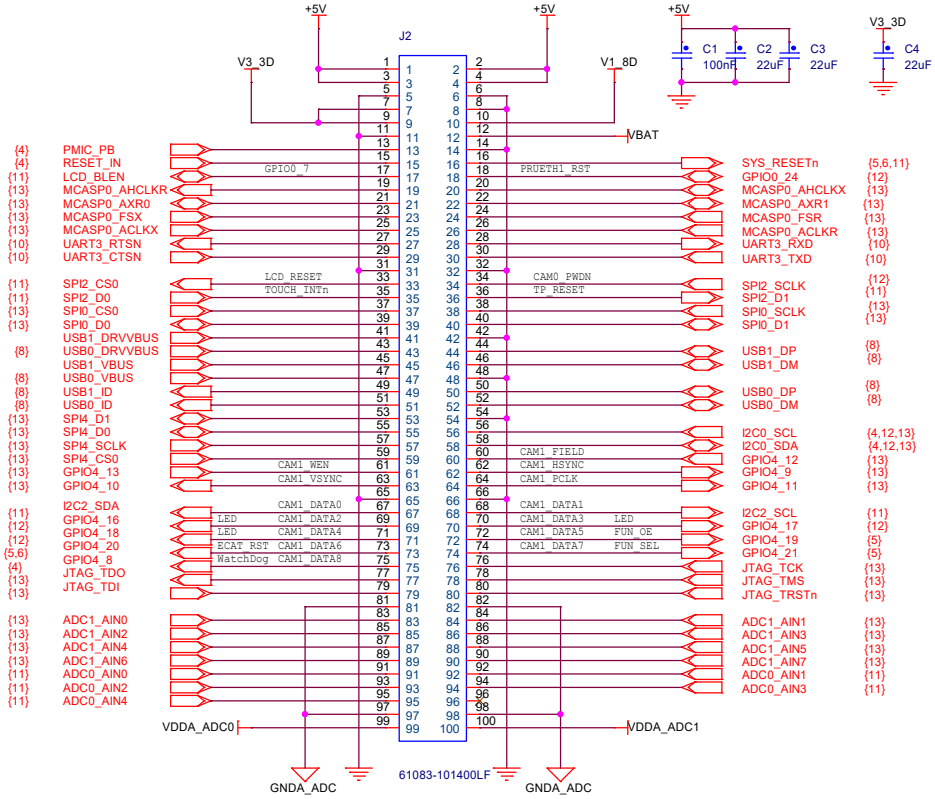

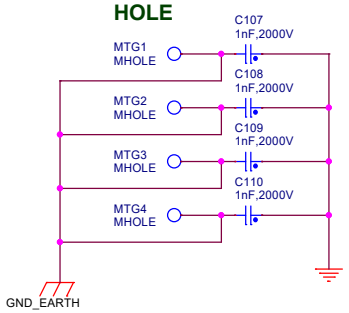

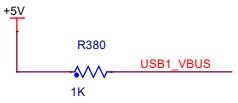

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Size: A3	Document Number: Connector	Rev: V1.1
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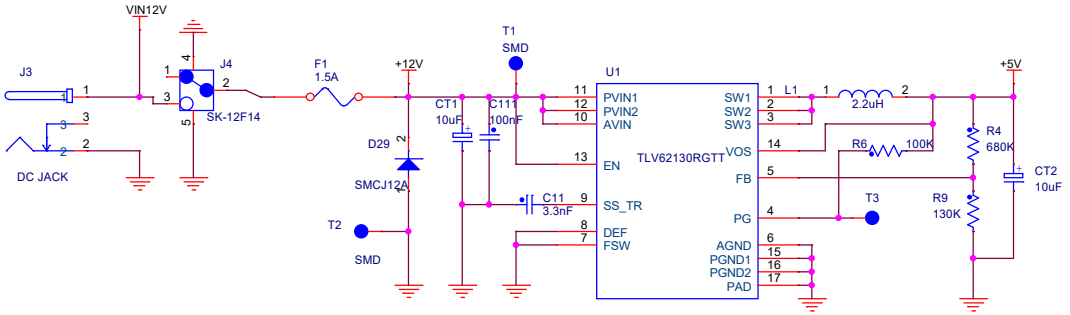
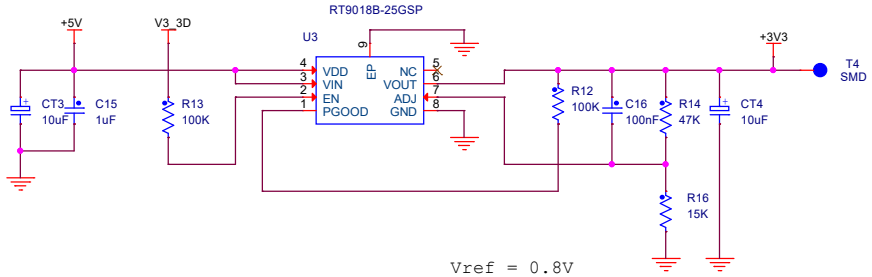
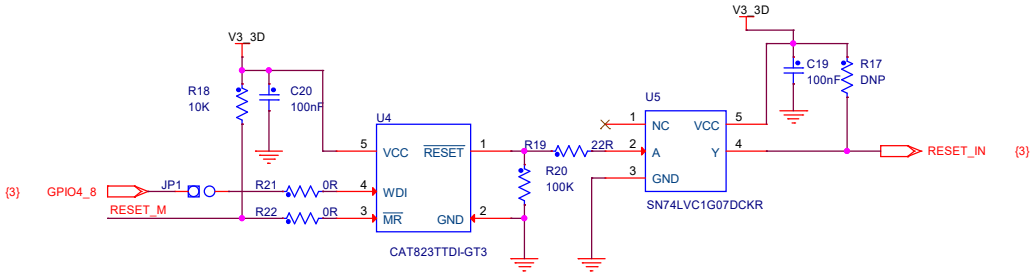


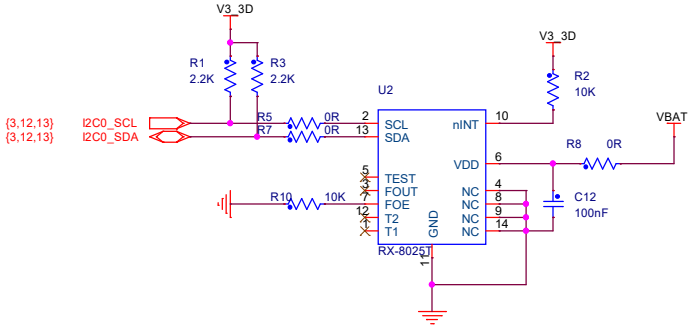
5~17V Vin convert to 5V/3A out
Vref = 0.8V

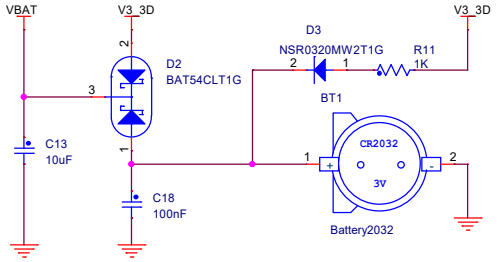


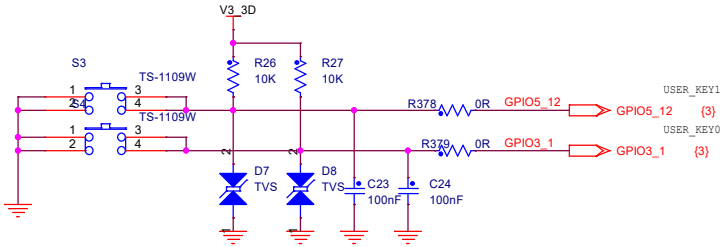
Vref = 0.8V

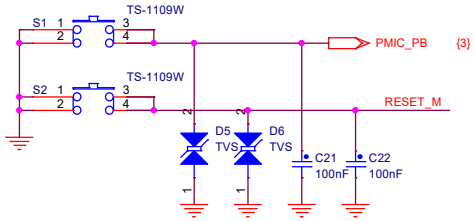


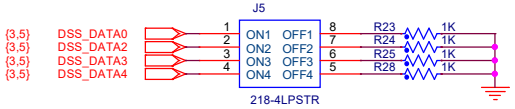
WD Timer peroid is 1.12S.











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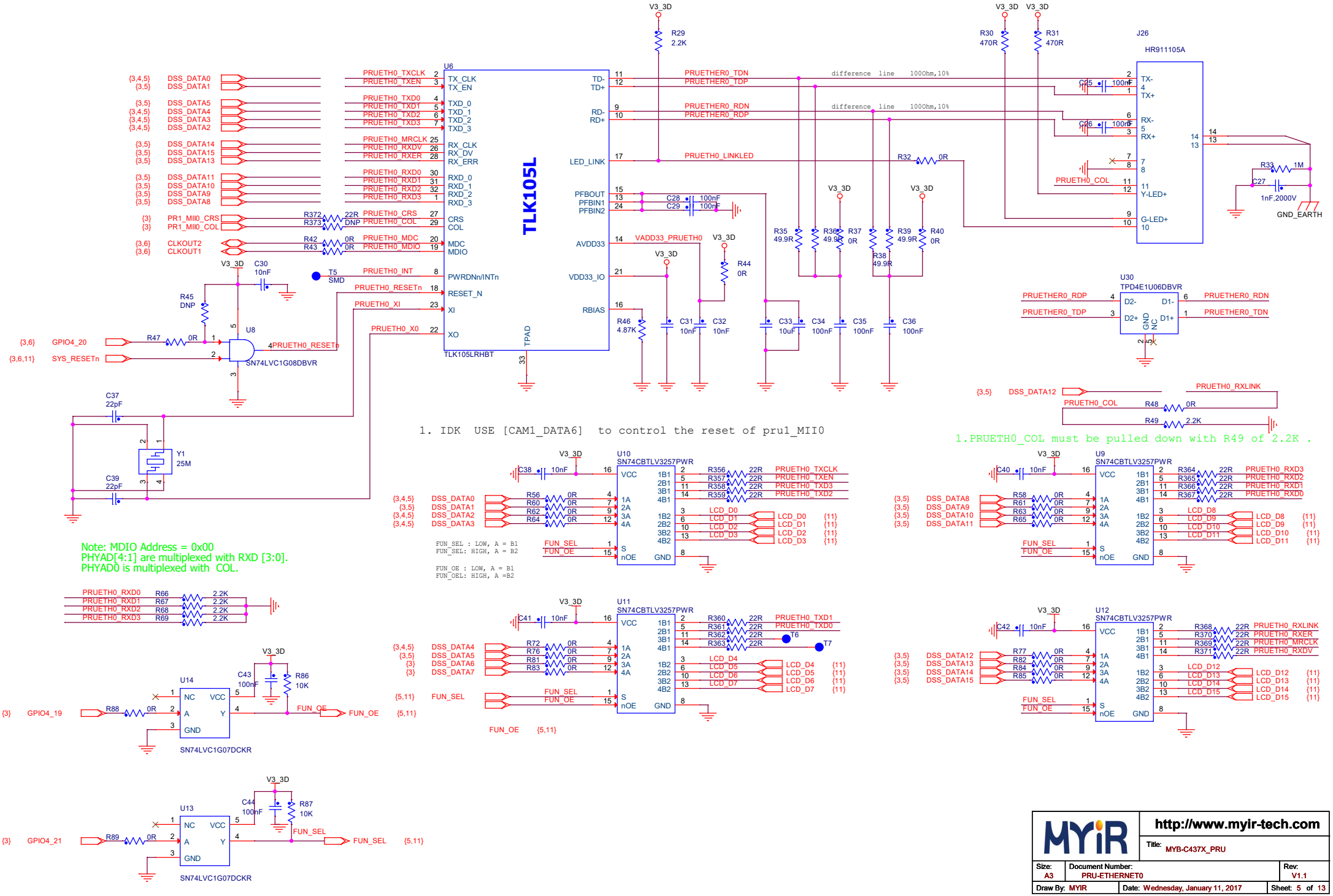
Title: MYB-C437X_PRU		
Size: A3	Document Number: Power Supply PMIC	Rev: V1.1
Draw By: MYIR	Date: Wednesday, January 11, 2017	Sheet: 4 of 13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TLK105L
TLK105LRHBT
U8
SN74LVC1G08DBVR
U10
SN74CBTLV3257PWR
U11
SN74CBTLV3257PWR
U9
SN74CBTLV3257PWR
U12
SN74CBTLV3257PWR
U14
SN74LVC1G07DCKR
U13
SN74LVC1G07DCKR
U30
TPD4E1U06DBVR
J26
HR911105A
V3_3D
PRUETH0_TXCLK
PRUETH0_TXEN
PRUETH0_TXD0
PRUETH0_TXD1
PRUETH0_TXD2
PRUETH0_TXD3
PRUETH0_MRCLK
PRUETH0_RXDV
PRUETH0_RXER
PRUETH0_RXD0
PRUETH0_RXD1
PRUETH0_RXD2
PRUETH0_RXD3
PRUETH0_CRS
PRUETH0_COL
PRUETH0_MDC
PRUETH0_MDIO
PRUETH0_INT
PRUETH0_RESETn
PRUETH0_XI
PRUETH0_X0
PRUETHER0_TDN
PRUETHER0_TDP
PRUETHER0_RDN
PRUETHER0_RDP
PRUETH0_LINKLED
VADD33_PRUETH0
DSS_DATA0
DSS_DATA1
DSS_DATA2
DSS_DATA3
DSS_DATA4
DSS_DATA5
DSS_DATA6
DSS_DATA7
DSS_DATA8
DSS_DATA9
DSS_DATA10
DSS_DATA11
DSS_DATA12
DSS_DATA13
DSS_DATA14
DSS_DATA15
PR1_MII0_CRS
PR1_MII0_COL
CLKOUT2
CLKOUT1
GPIO4_20
SYS_RESETn
GPIO4_19
GPIO4_21
LCD_D0
LCD_D1
LCD_D2
LCD_D3
LCD_D4
LCD_D5
LCD_D6
LCD_D7
LCD_D8
LCD_D9
LCD_D10
LCD_D11
LCD_D12
LCD_D13
LCD_D14
LCD_D15
FUN_SEL
FUN_OE
PRUETH0_RXLINK
PRUETH0_RXER
PRUETH0_MRCLK
PRUETH0_RXDV
difference line 100Ohm,10%
GND_EARTH
1. IDK USE [CAM1_DATA6] to control the reset of pru1_MII0
1.PRUETH0_COL must be pulled down with R49 of 2.2K .
Note: MDIO Address = 0x00
PHYAD[4:1] are multiplexed with RXD [3:0].
PHYAD0 is multiplexed with COL.
FUN_SEL : LOW, A = B1
FUN_SEL: HIGH, A = B2
FUN_OE : LOW, A = B1
FUN_OEL: HIGH, A =B2
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Size: A3
Document Number: PRU-ETHERNET0
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Date: Wednesday, January 11, 2017
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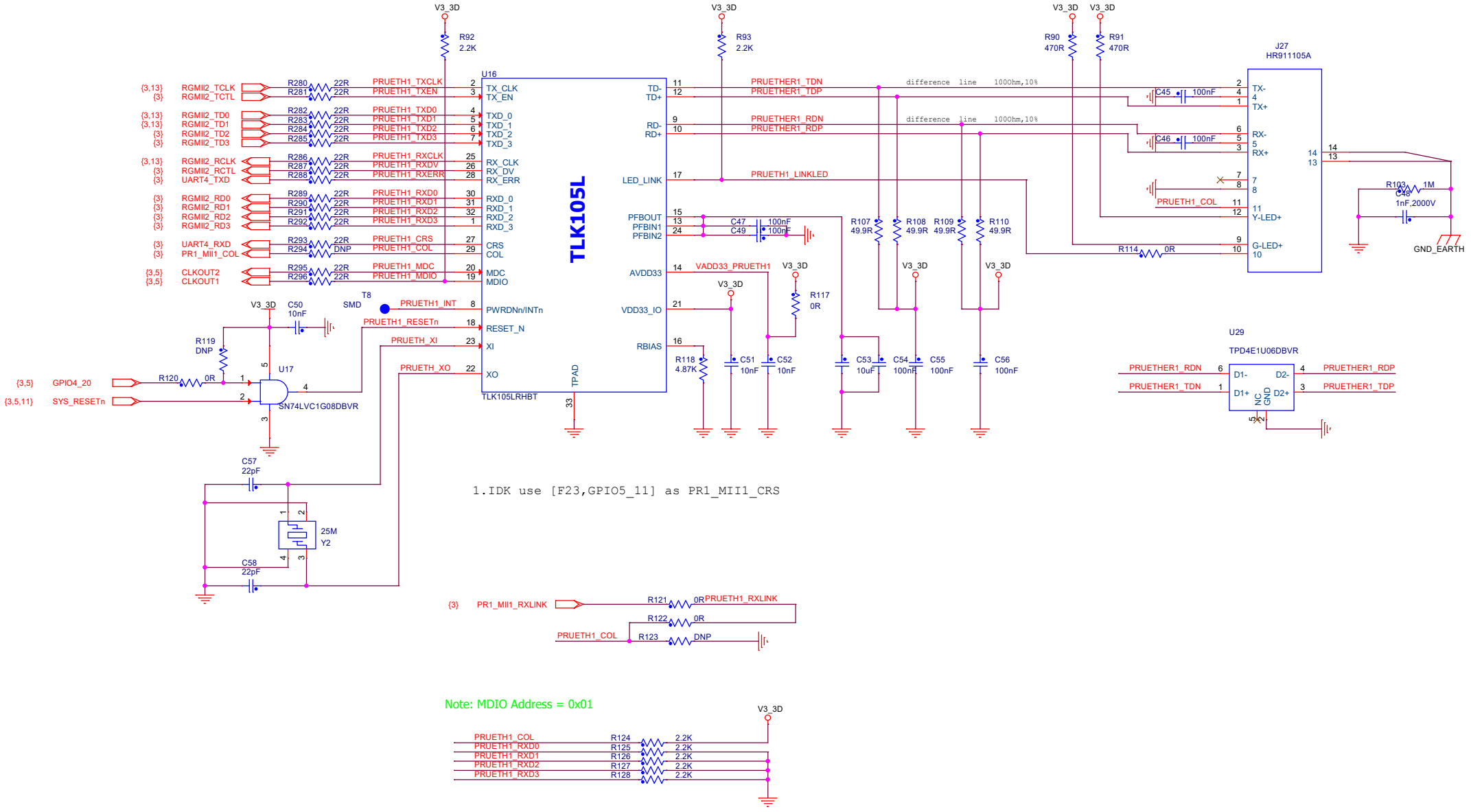

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	Title: MYB-C437X_PRU	
Size: A3	Document Number: PRU-ETHERNET1	Rev: V1.1
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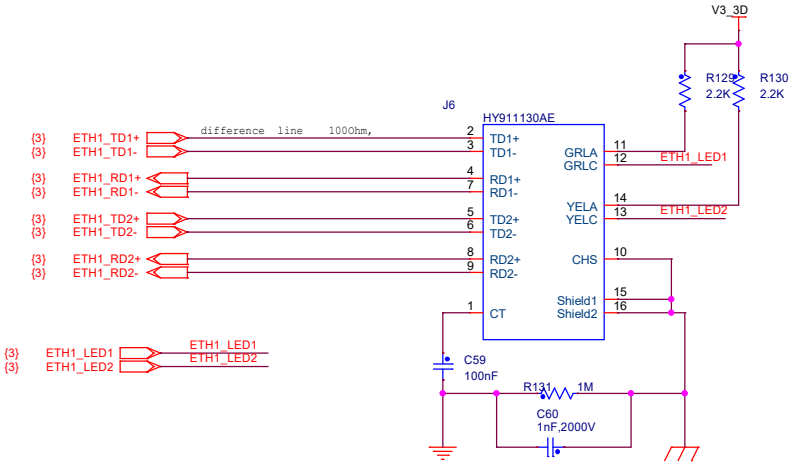

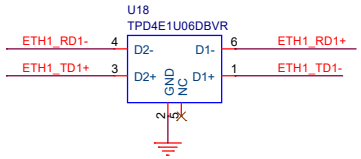

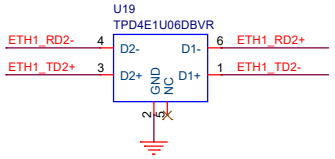

MDIO_CLK was pulled up with 10K to 3.3 voltage.
MDIO_DATA was pulled up with 1.5K to 3.3 voltage.
PHY Address :100

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	Title: MYB-C437X_PRU	
Size: A3	Document Number: Ethernet	Rev: V1.1
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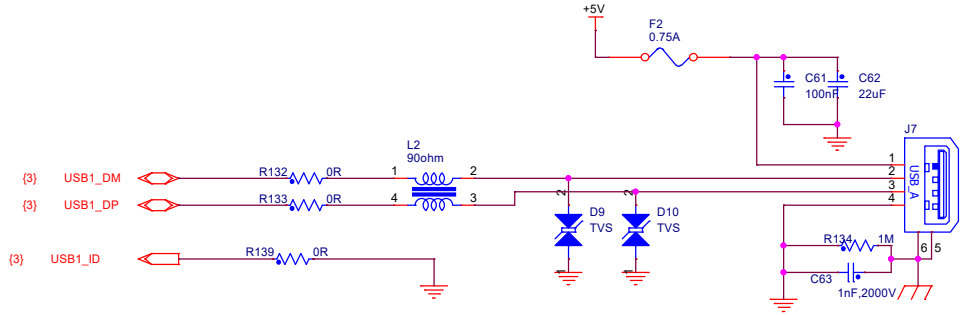

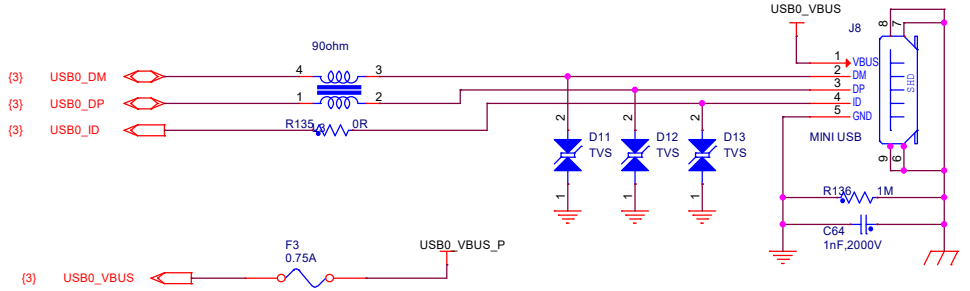

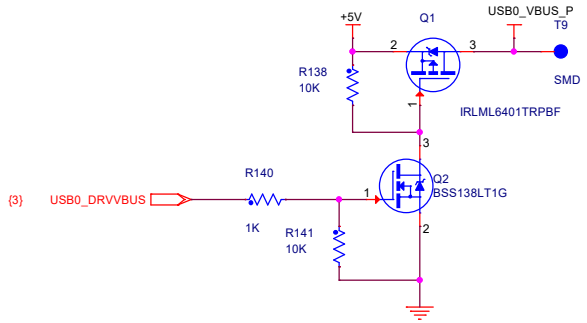

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	Title: MYB-C437X_PRU	
Size: A3	Document Number: USB Port	Rev: V1.1
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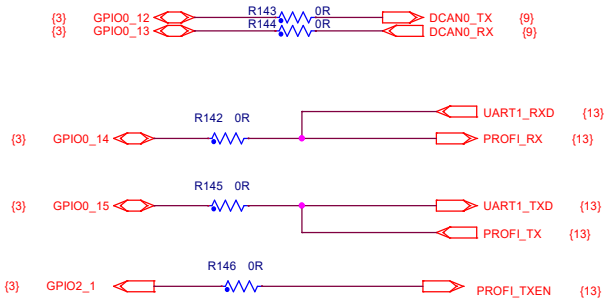
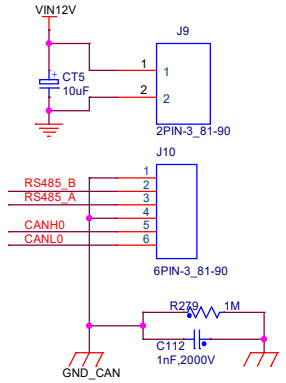
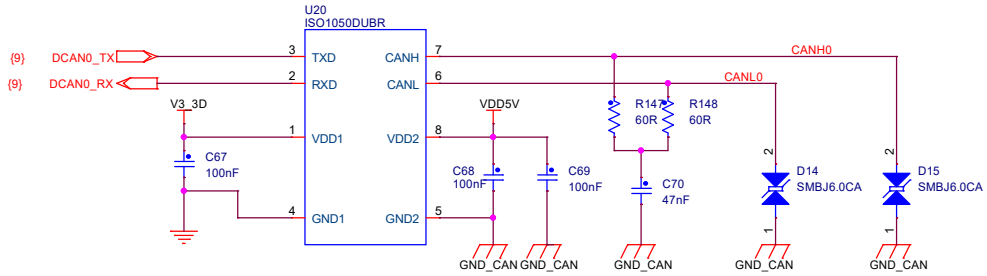


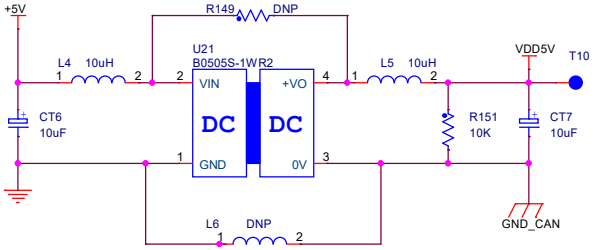
PROFIBUS: PRU1_UART0 (TX, RX)



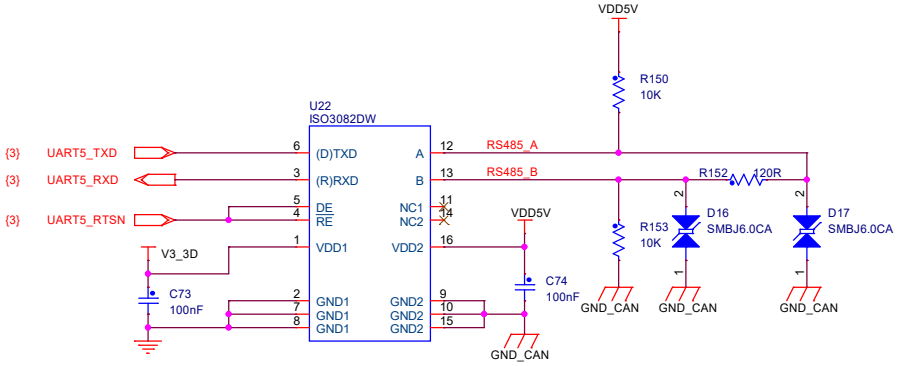
CAN



POWER



RS485



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Size: A3	Document Number: CAN,RS485	Rev: V1.1
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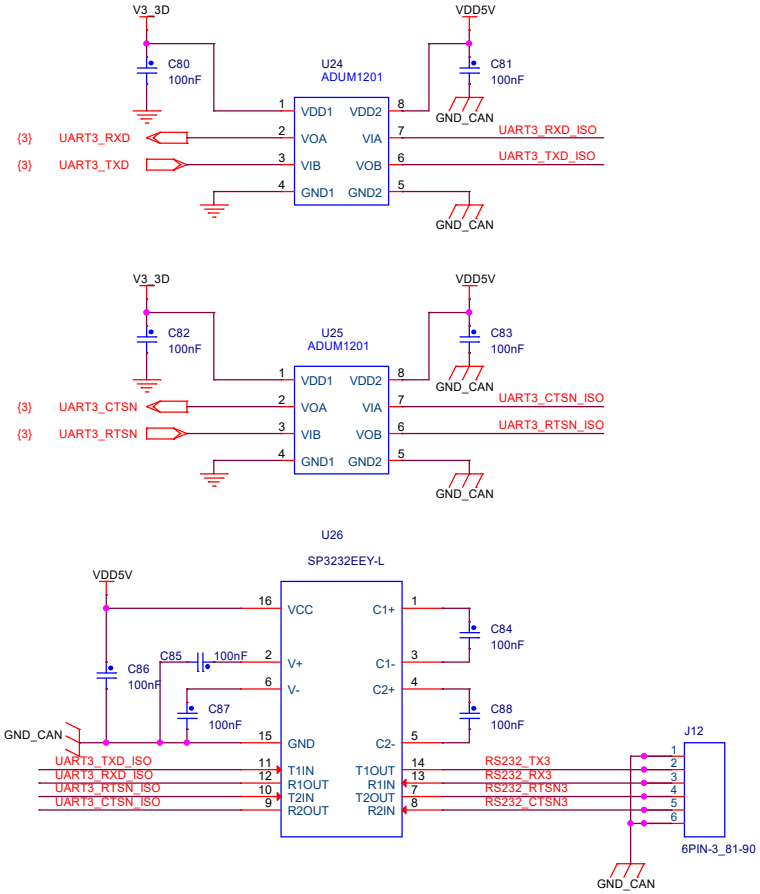
RS232



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	Title: MYB-C437X_PRU	
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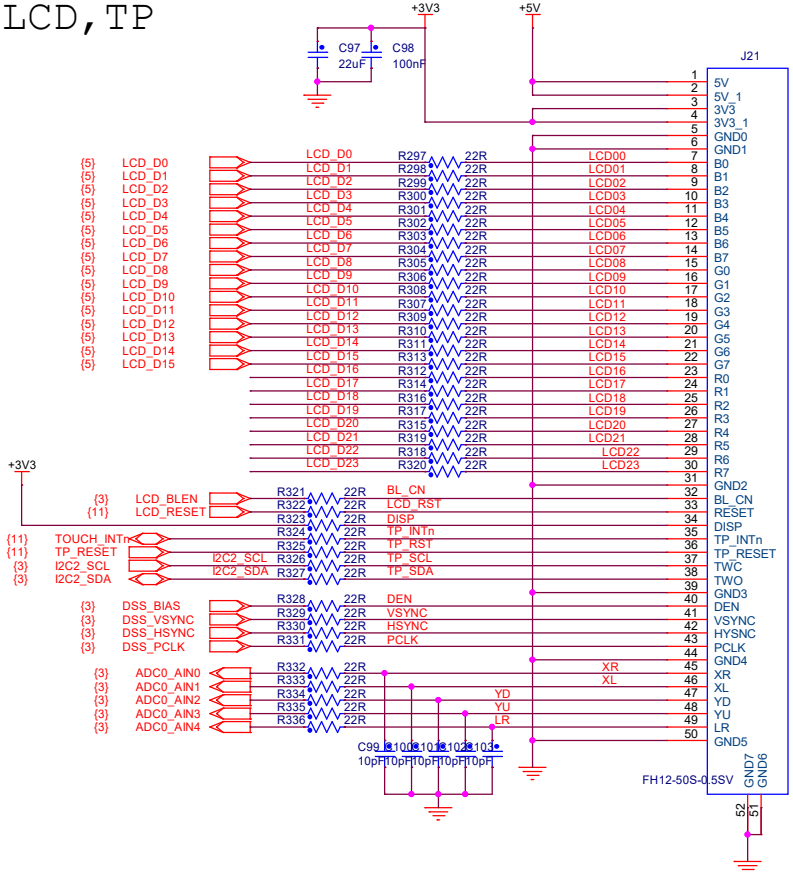
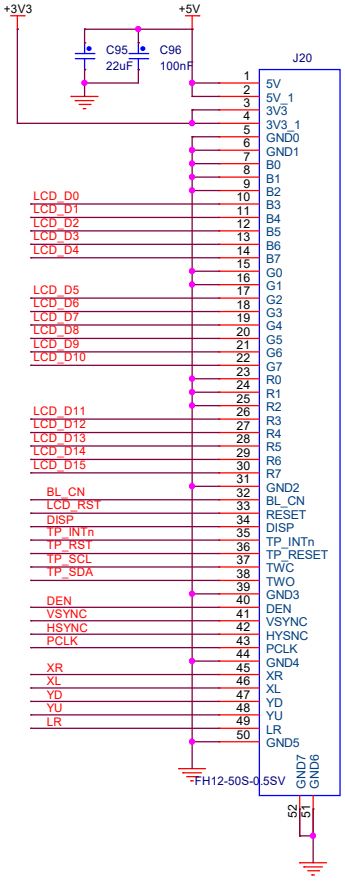
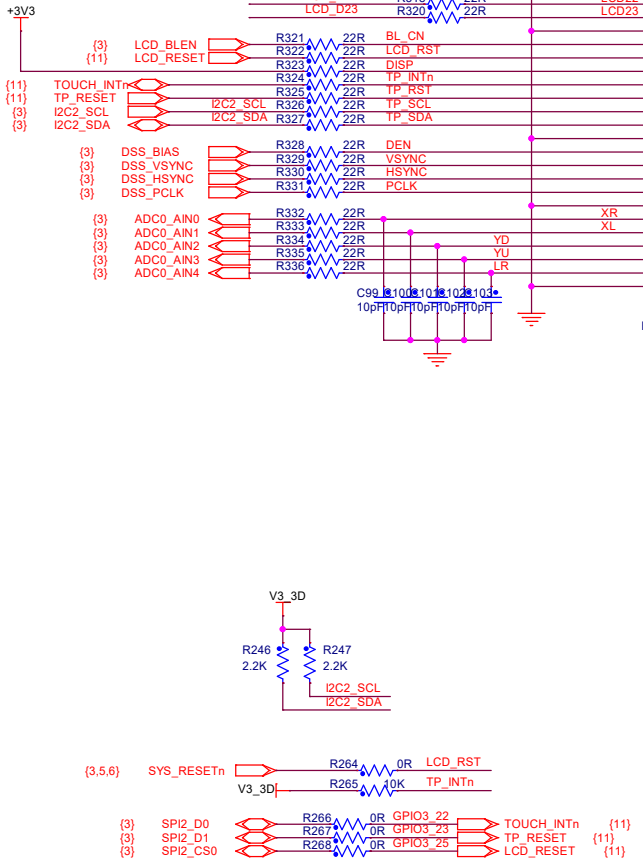
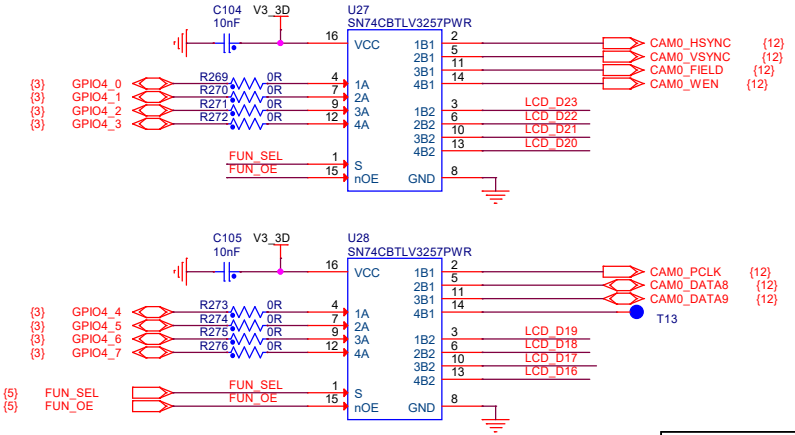
LCD,TP







GPIO Reuse



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Size: A3	Document Number: LCD,SYSBOOT	Rev: V1.0
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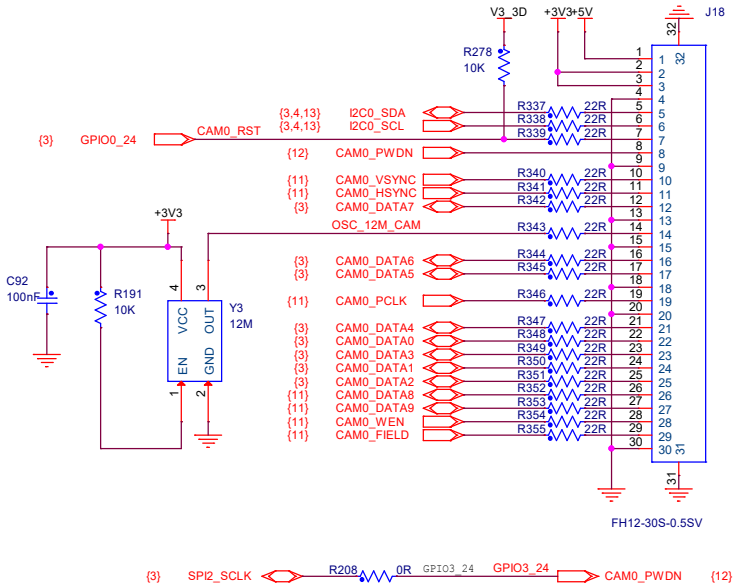
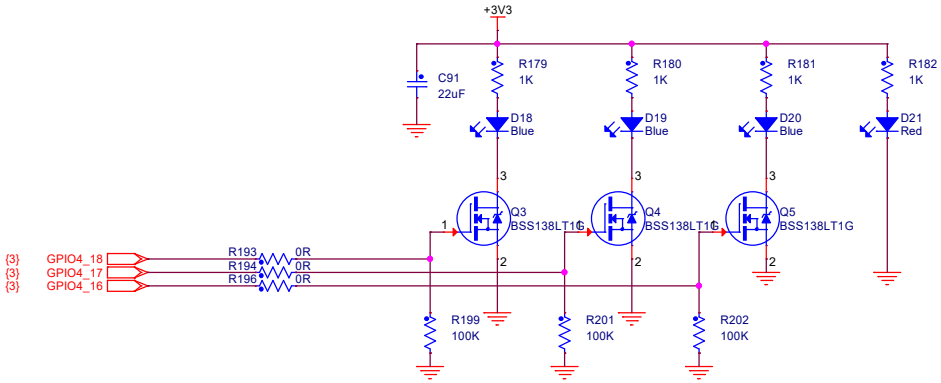
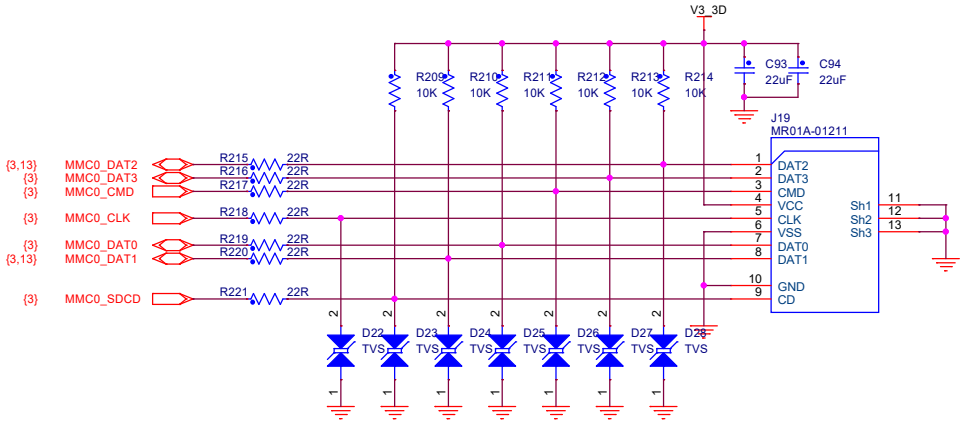
Camera



LED



TF Card



MYiR http://www.myir-tech.com	Title: MYB-C437X_PRU	
Size: A3	Document Number: CAMERA,SD,LED	Rev: V1.1
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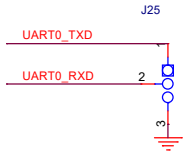
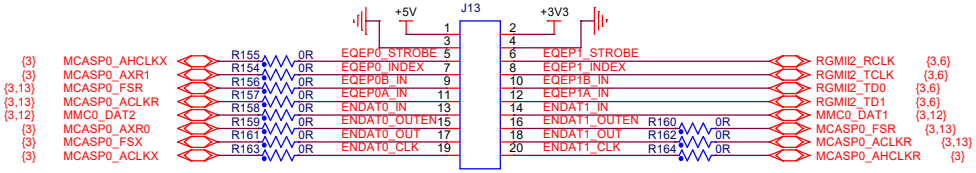
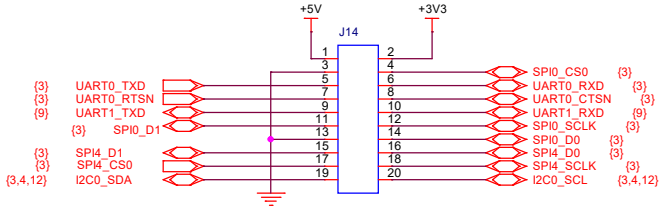
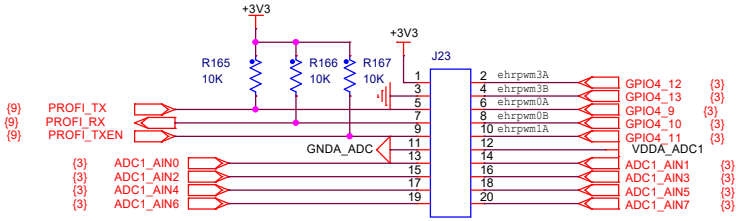
UART0 for Debug information



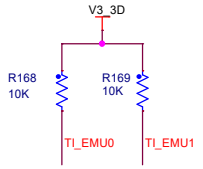
Expand Port

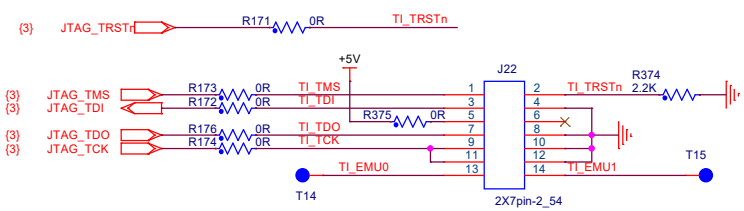






TI -JTAG





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